



N-Channel Depletion-Mode Vertical DMOS FET in Single and Dual Options

Features

- ▶ Very low gate threshold voltage
- ▶ Designed to be source-driven
- ▶ Low switching losses
- ▶ Low effective output capacitance
- ▶ Designed for inductive loads
- ▶ Well matched for low second harmonic when driven by Supertex MD2130

Applications

- ▶ Medical ultrasound beamforming
- ▶ Ultrasonic array focusing transmitter
- ▶ Piezoelectric transducer waveform drivers
- ▶ High speed arbitrary waveform generator
- ▶ Normally-on switches
- ▶ Solid state relays
- ▶ Constant current sources
- ▶ Power supply circuits

General Description

The Supertex DN2625 is a low threshold depletion-mode (normally-on) transistor utilizing an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

The DN2625DK6-G contains two MOSFETs in an 8-lead, dual pad DFN package. The DN2625K6-G in the 14-lead QFN package is not recommended for new designs, but may continue to be purchased for existing designs.

Ordering Information

| Device | Package Options | | | BV _{DSX} / BV _{DGX} (V) | V _{GS(OFF)} (max) (V) | I _{DS} (pulsed) (V _{GS} = 0.9V) (min) (A) |
|--------|-------------------|----------------------------------------------------------------------------------|-------------------------------------------------------------------------|----------------------------------------------|--------------------------------------|-------------------------------------------------------------------------|
| | TO-252 (D-PAK) | 8-Lead DFN 5.00x5.00mm body 0.90mm height (max) 1.27mm pitch (dual pad) | 14-Lead QFN* 5.00x5.00mm body 1.00mm height (max) 1.27mm pitch | | | |
| DN2625 | DN2625K4-G | DN2625DK6-G | DN2625K6-G | 250 | -2.1 | 3.3 |

-G indicates package is RoHS compliant ('Green')

* This package obsolete. For single MOSFETs use the TO-252 D-PAK (K4), for dual MOSFETs use the 8-Lead DFN (K6) (dual pad).



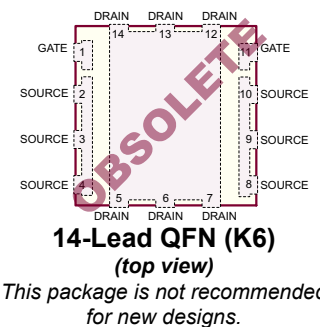
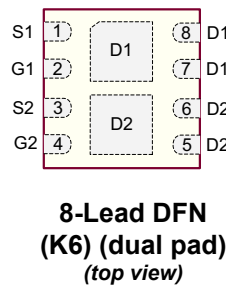
Absolute Maximum Ratings

| Parameter | Value |
|-----------------------------------|-----------------|
| Drain-to-source voltage | 250V |
| Drain-to-gate voltage | 250V |
| Gate-to-source voltage | ±20V |
| Operating and storage temperature | -55°C to +150°C |
| Soldering temperature* | 300°C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* Distance of 1.6mm from case for 10 seconds.

Pin Configurations



Product Marking

Packages may or may not include the following marks: Si or 

Si YYWW
DN2625
LLLLLLL
YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

TO-252 D-PAK (K4)

D2625D
LLLLLL
YYWW
AAACCC
L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
_____ = "Green" Packaging

8-Lead DFN (K6) (dual pad)

DN2625
LLLLLL
YYWW
AAACCC
L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
_____ = "Green" Packaging

14-Lead QFN (K6)

This package is not recommended for new designs.

Thermal Characteristics

| Package | I_D (continuous) ¹ (A) | I_D (pulsed) (A) | $R_{\theta ja}$ (°C/W) | $R_{\theta jc}$ (°C/W) | I_{DR}^1 (A) | I_{DRM} (A) |
|-----------------------|-------------------------------------------|--------------------------|---------------------------|---------------------------|-------------------|------------------|
| D-PAK | 1.1 | 3.3 | 50 ² | 5.5 | 1.1 | 3.3 |
| 8-Lead DFN (dual pad) | 1.1 | 3.3 | 32 ³ | 3.2 | 1.1 | 3.3 |
| 14-Lead QFN | 1.1 | 3.3 | 22 ³ | 2.0 ⁴ | 1.1 | 3.3 |

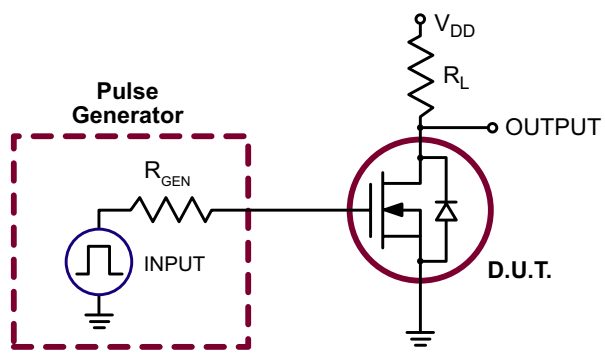
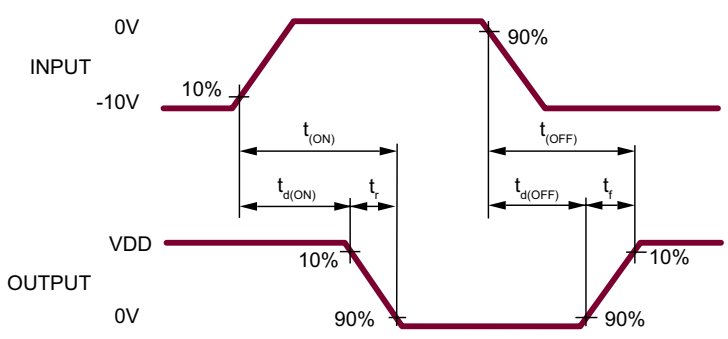
Notes:

- I_D (Continuous) is limited by max. T_j
- 4-layer, 1oz, 3x4inch PCB, with 20-via for drain pad.
- 4-layer, 1oz, 3x4inch PCB, with 12-via for drain pad.
- Junction to the DFN thermal pad.

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

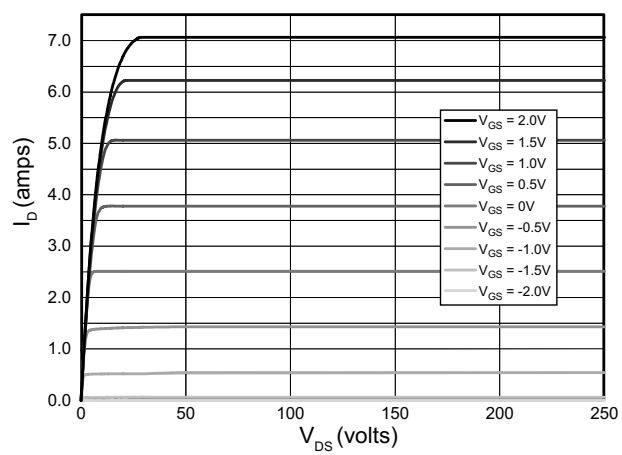
| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|----------------------|------------------------------------------|------|-----|-------|----------|-----------------------------------------------------------------------------------------------|
| BV_{DSX} | Drain-to-source breakdown voltage | 250 | - | - | V | $V_{GS} = -2.5V, I_D = 50\mu A$ |
| BV_{DGX} | Drain-to-gate breakdown voltage | 250 | - | - | V | $V_{GS} = -2.5V, I_D = 50\mu A$ |
| $V_{GS(OFF)}$ | Gate-to-source off voltage | -1.5 | - | -2.1 | V | $V_{DS} = 15V, I_D = 100\mu A$ |
| $\Delta V_{GS(OFF)}$ | Change in $V_{GS(OFF)}$ with temperature | - | - | -4.5 | mV/°C | $V_{DS} = 15V, I_D = 100\mu A$ |
| I_{GSS} | Gate body leakage current | - | - | 100 | nA | $V_{GS} = \pm 20V, V_{DS} = 0V$ |
| $I_{D(OFF)}$ | Drain-to-source leakage current | - | - | 1.0 | μA | $V_{DS} = 250V, V_{GS} = -5.0V$ |
| | | - | - | 200 | | $V_{DS} = 250V, V_{GS} = -5.0V, T_A = 125^\circ\text{C}$ |
| I_{DSS} | Saturated drain-to-source current | 1.1 | - | - | A | $V_{GS} = 0V, V_{DS} = 15V$ |
| $I_{DS(PULSE)}$ | Pulsed drain-to-source current | 3.1 | 3.3 | - | A | $V_{GS} = 0.9V, V_{DS} = 15V$ (with duty cycle of 1%) |
| $R_{DS(ON)}$ | Static drain-to-source on-resistance | - | - | 3.5 | Ω | $V_{GS} = 0V, I_D = 1.0A$ |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with temperature | - | - | 1.1 | %/°C | $V_{GS} = 0V, I_D = 200mA$ |
| G_{FS} | Forward transconductance | 100 | - | - | mmho | $V_{DS} = 10V, I_D = 150mA$ |
| C_{ISS} | Input capacitance | - | 800 | 1000 | pF | $V_{GS} = -2.5V,$ $V_{DS} = 25V,$ $f = 1.0MHz$ |
| C_{OSS} | Common source output capacitance | - | 70 | 210 | | |
| C_{RSS} | Reverse transfer capacitance | - | 18 | 70 | | |
| $t_{d(ON)}$ | Turn-on delay time | - | - | 10 | ns | $V_{DD} = 25V,$ $I_D = 150mA,$ $R_{GEN} = 3.0\Omega,$ $V_{GS} = 0v \text{ to } -10V$ |
| t_r | Rise time | - | - | 20 | | |
| $t_{d(OFF)}$ | Turn-off delay time | - | - | 10 | | |
| t_f | Fall time | - | - | 20 | | |
| V_{SD} | Diode forward voltage drop | - | - | 1.8 | V | $V_{GS} = -2.5V, I_{SD} = 150mA$ |
| Q_G | Total gate charge | - | - | 7.04 | nC | $I_D = 3.5A,$ $V_{DS} = 100V,$ $V_{GS} = 1.5V$ |
| Q_{GS} | Gate-to-source charge | - | - | 0.783 | | |
| Q_{GD} | Gate-to-drain charge | - | - | 3.73 | | |

Switching Waveforms and Test Circuit

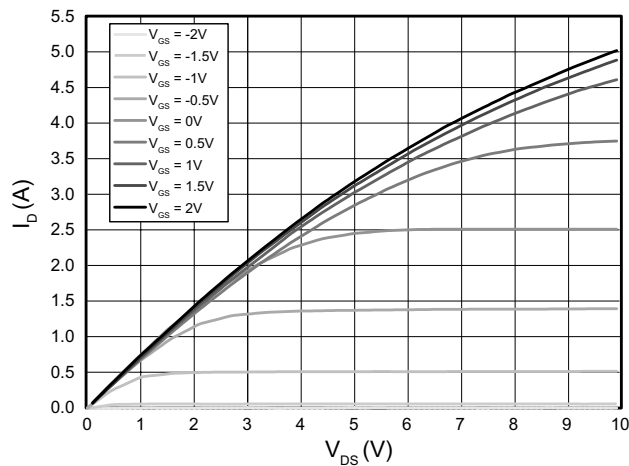


Typical Performance Curves

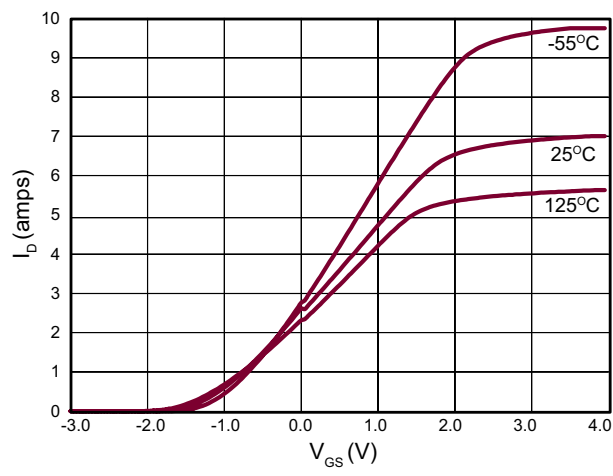
Output Characteristics



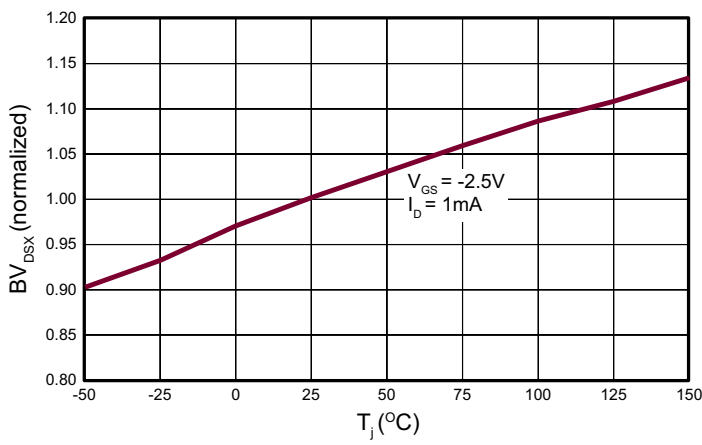
Saturation Characteristics



Transfer Characteristics

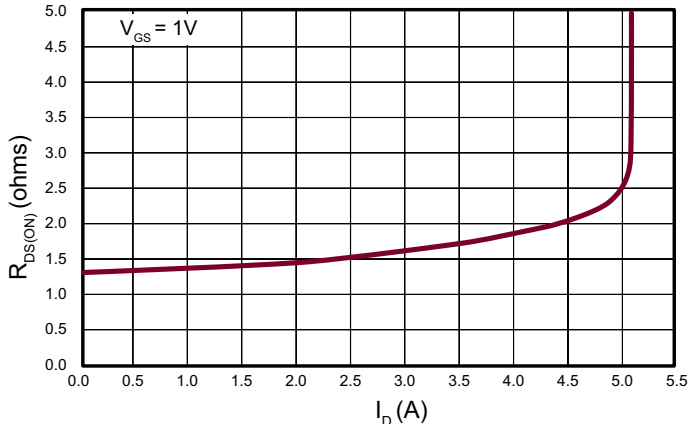


BV_DSX Variation With Temperature

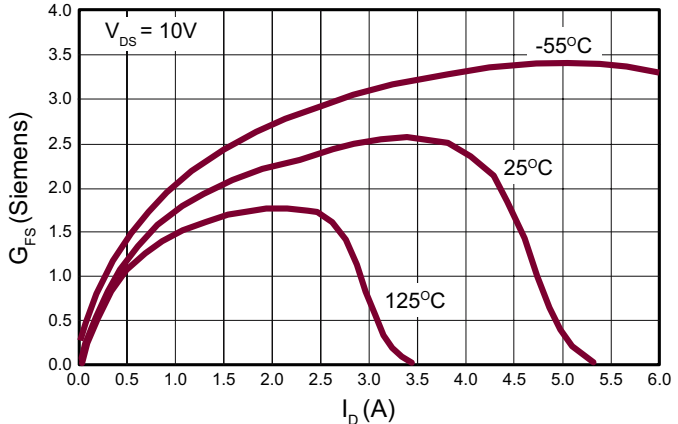


Typical Performance Curves (cont.)

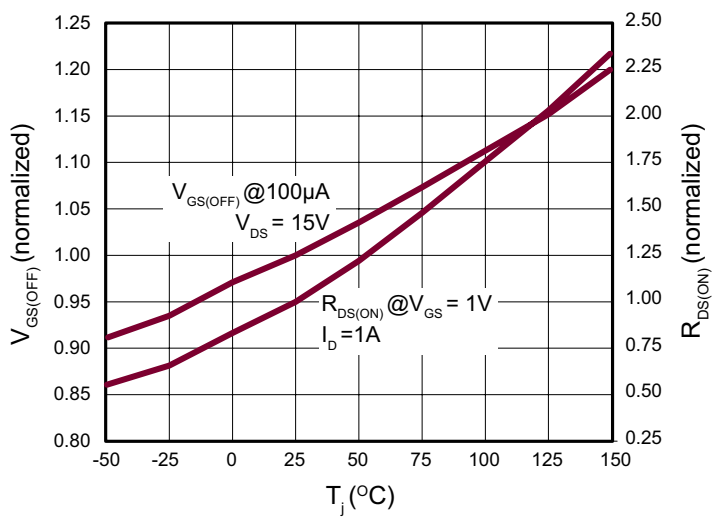
On-Resistance vs Drain Current



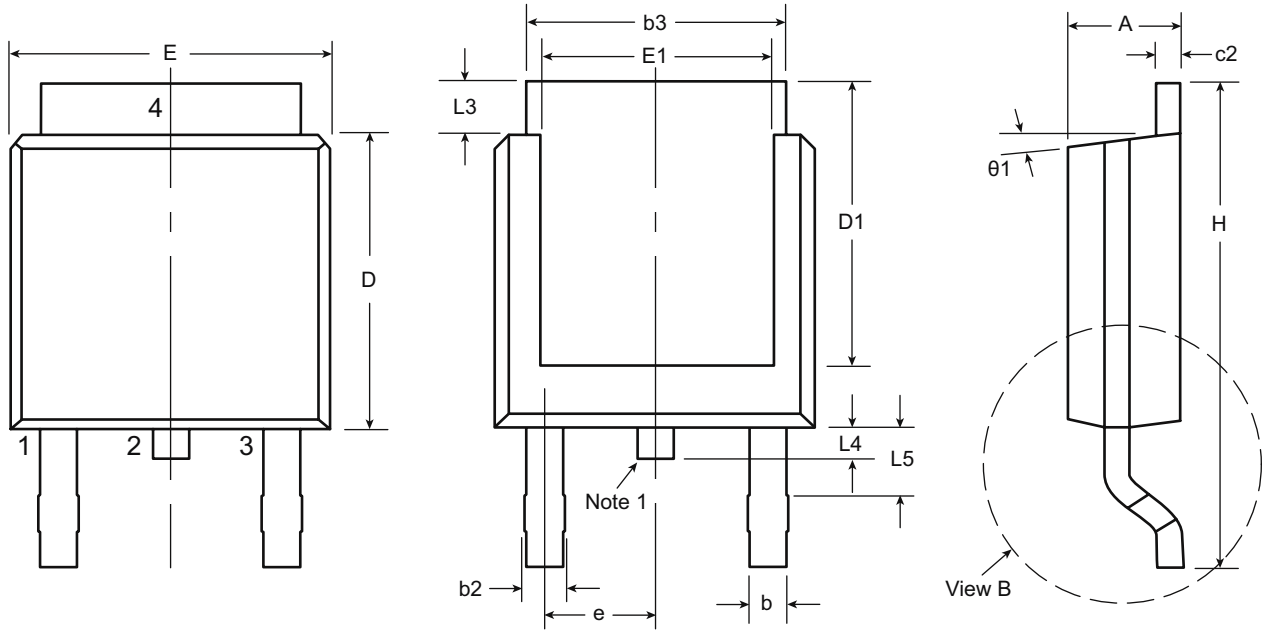
Transconductance vs Drain Current



$V_{GS(OFF)}$ and $R_{DS(ON)}$ Variation With Temperature



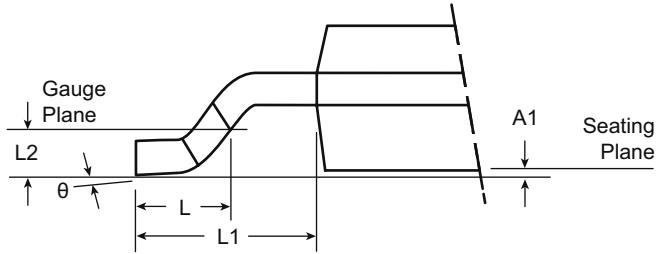
3-Lead TO-252 D-PAK Package Outline (K4)



Front View

Rear View

Side View



View B

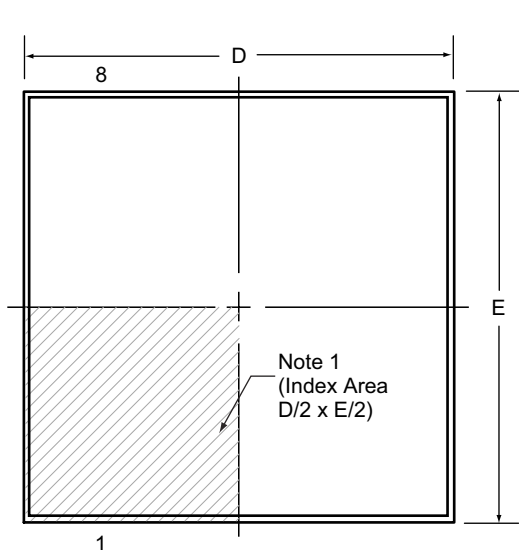
Note:
 1. Although 4 terminal locations are shown, only 3 are functional. Lead number 2 was removed.

| Symbol | A | A1 | b | b2 | b3 | c2 | D | D1 | E | E1 | e | H | L | L1 | L2 | L3 | L4 | L5 | θ | θ1 | |
|--------------------|-----|------|-------|------|------|------|------|------|-------|------|----------|------|------|----------|----------|------|-------|------|------|------|-----|
| Dimension (inches) | MIN | .086 | .000* | .025 | .030 | .195 | .018 | .235 | .205 | .250 | .170 | .370 | .055 | .108 REF | .020 BSC | .035 | .025* | .045 | 0° | 0° | |
| | NOM | - | - | - | - | - | .240 | - | - | - | .090 BSC | - | .060 | | | - | - | - | - | - | - |
| | MAX | .094 | .005 | .035 | .045 | .215 | .035 | .245 | .217* | .265 | .182* | .410 | .070 | | | - | - | .050 | .040 | .060 | 10° |

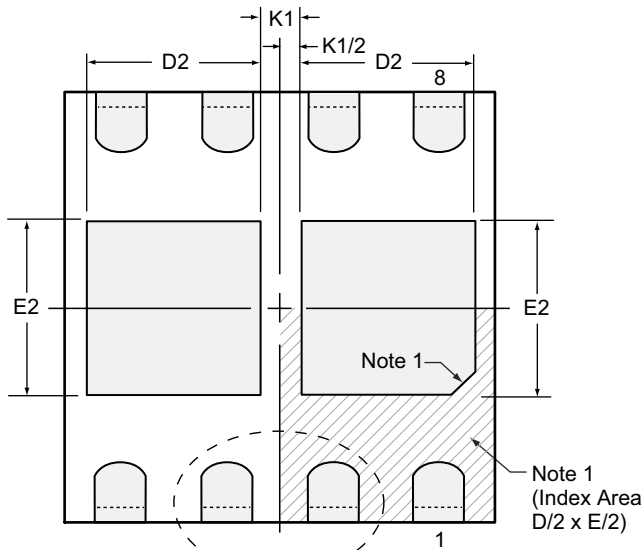
JEDEC Registration TO-252, Variation AA, Issue E, June 2004.
 * This dimension is not specified in the JEDEC drawing.
Drawings not to scale.
 Supertex Doc. #: DSPD-3TO252K4, Version E041309.

8-Lead DFN Package Outline (K6)

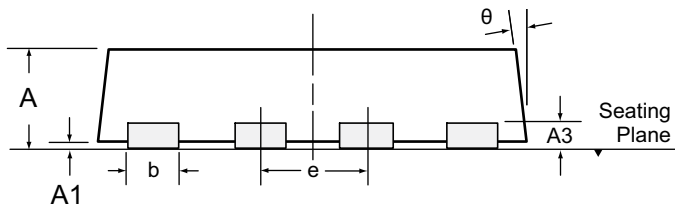
5.00x5.00mm body, 0.90mm height (max), 1.27mm pitch (dual pad)



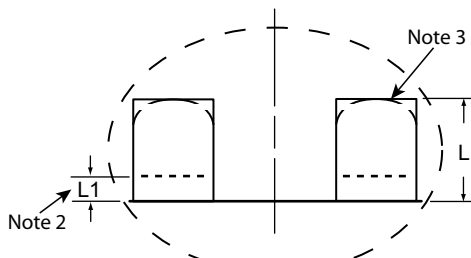
Top View



Bottom View



Side View



View B

Notes:

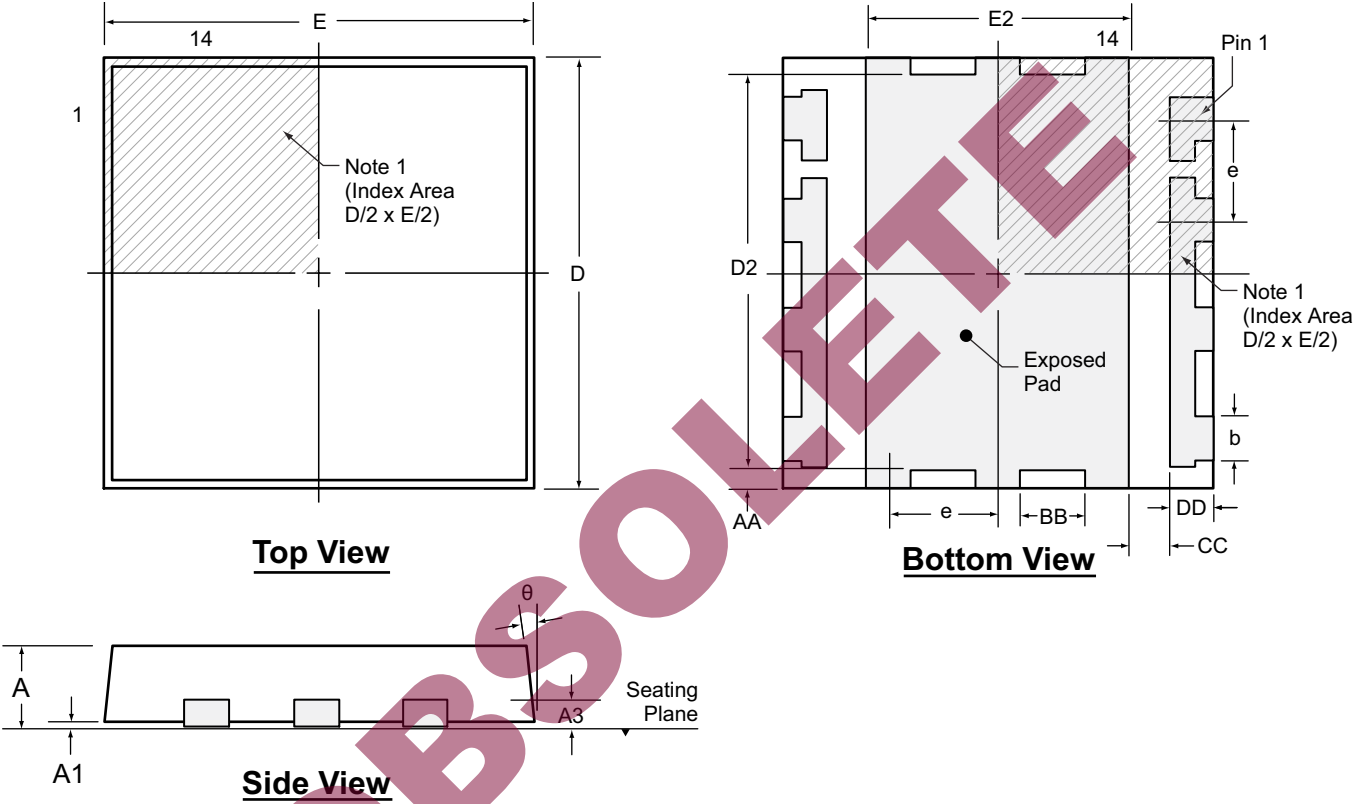
1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

| Symbol | A | A1 | A3 | b | D | D2 | E | E2 | e | K1 | L | L1 | θ | |
|----------------|-----|------|------|----------|------|------|------|------|------|----------|----------|------|------|-----|
| Dimension (mm) | MIN | 0.80 | 0.00 | 0.20 REF | 0.35 | 4.90 | 1.93 | 4.90 | 1.90 | 1.27 BSC | 0.40 REF | 0.40 | 0.00 | 0° |
| | NOM | 0.85 | - | | 0.40 | 5.00 | 2.03 | 5.00 | 2.00 | | | 0.50 | - | - |
| | MAX | 0.90 | 0.05 | | 0.45 | 5.10 | 2.13 | 5.10 | 2.10 | | | 0.60 | 0.15 | 14° |

Drawings not to scale

Supertex Doc. #: DSPD-8DFNK65x5P127, Version A040209

14-Lead QFN Package Outline (K6)
5.00x5.00mm body, 1.00mm height (max), 1.27mm pitch



Notes:

- 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol | A | A1 | A3 | b | D | D2 | E | E2 | e | AA | BB | CC | DD | θ | |
|----------------|-----|------|------|----------|------|------|------|------|------|----------|-------|-------|------|----------|-----|
| Dimension (mm) | MIN | 0.80 | 0.00 | 0.20 REF | 0.46 | 4.85 | 4.45 | 4.85 | 2.52 | 1.27 BSC | 0.152 | 0.473 | 0.66 | 0.456 | 0° |
| | NOM | 0.90 | 0.02 | | 0.51 | 5.00 | 4.50 | 5.00 | 2.57 | | 0.252 | 0.523 | 0.71 | 0.506 | - |
| | MAX | 1.00 | 0.05 | | 0.58 | 5.15 | 4.55 | 5.15 | 2.62 | | 0.352 | 0.583 | 0.77 | 0.566 | 14° |

Drawings not to scale.
 Supertex Doc. #: DSPD-14QFNK65X5P127, Version B090808.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

Supertex inc. does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." Supertex inc. does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the Supertex inc. (website: <http://www.supertex.com>)