Features:
• Output Voltage Resolutions:
  - 12-bit: MCP4726
  - 10-bit: MCP4716
  - 8-bit: MCP4706
• Rail-to-Rail Output
• Fast Settling Time of 6 µs (typical)
• DAC Voltage Reference Options:
  - VDD
  - VREF Pin
• Output Gain Options:
  - Unity (1x)
  - 2x, only when VREF pin is used as voltage source
• Nonvolatile Memory (EEPROM):
  - Auto Recall of Saved DAC register setting
  - Auto Recall of Saved Device Configuration (Voltage Reference, Gain, Power-Down)
• Power-Down modes:
  - Disconnects output buffer
  - Selection of VOUT pull-down resistors (640 kΩ, 125 kΩ, or 1 kΩ)
• Low-Power Consumption:
  - Normal Operation: 210 µA typical
  - Power-Down Operation: 60 nA typical (PD1:PD0 = 11)
• I²C™ Interface:
  - Eight Available Addresses
  - Standard (100 kbps), Fast (400 kbps), and High-Speed (3.4 Mbps) modes
• Small 6-lead SOT-23 and DFN (2x2) Packages
• Extended Temperature Range: -40°C to +125°C

Applications:
• Set Point or Offset Trimming
• Sensor Calibration
• Low-Power Portable Instrumentation
• PC Peripherals
• Data Acquisition Systems
• Motor Control

Package Types

Description:
The MCP4706/4716/4726 are single channel 8-bit, 10-bit, and 12-bit buffered voltage output Digital-to-Analog Converters (DAC) with nonvolatile memory and an I²C serial interface. This family will also be referred to as MCP47X6.

The VREF pin or the device VDD can be selected as the DAC’s reference voltage. When VDD is selected, VDD is connected internally to the DAC reference circuit. When the VREF pin is used, the user can select the output buffer’s gain to 1 or 2. When the gain is 2, the VREF pin voltage should be limited to a maximum of VDD/2.

The DAC register value and Configuration bits can be programmed to nonvolatile memory (EEPROM). The nonvolatile memory holds the DAC register and Configuration bit values when the device is powered off. A device Reset (such as a Power-on Reset) latches these stored values into the volatile memory.

Power-Down modes enable system current reduction when the DAC output voltage is not required. The VOUT pin can be configured to present a low, medium, or high resistance load.

These devices have a two-wire I²C™ compatible serial interface for standard (100 kHz), fast (400 kHz), or High-Speed (3.4 MHz) mode.

These devices are available in small 6-pin SOT-23 and DFN 2x2 mm packages.
Block Diagram
1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

| Voltage on V<sub>DD</sub> with respect to V<sub>SS</sub> | -0.6V to +6.5V |
| Voltage on all pins with respect to V<sub>SS</sub> | -0.3V to V<sub>DD</sub> + 0.3V |
| Input clamp current, I<sub>IK</sub> (V<sub>i</sub> < 0, V<sub>i</sub> > V<sub>DD</sub>) | ±20 mA |
| Output clamp current, I<sub>OK</sub> (V<sub>o</sub> < 0 or V<sub>o</sub> > V<sub>DD</sub>) | ±20 mA |
| Maximum input current source/sunk by SDA, SCL pins | 2 mA |
| Maximum output current sunk by SDA Output pin | 25 mA |
| Maximum current out of V<sub>SS</sub> pin | 50 mA |
| Maximum current into V<sub>DD</sub> pin | 50 mA |
| Maximum current sourced by the V<sub>OUT</sub> pin | 40 mA |
| Maximum current sunk by the V<sub>OUT</sub> pin | 40 mA |
| Maximum current sunk by the V<sub>REF</sub> pin | 40 µA |

Package power dissipation (T<sub>A</sub> = +50°C, T<sub>J</sub> = +150°C)

| SOT-23-6 | 452 mW |
| DFN-6 | 1098 mW |

Storage temperature | -65°C to +150°C |
Ambient temperature with power applied | -55°C to +125°C |
ESD protection on all pins | ≥ 6 kV (HBM) |
| | ≥ 400V (MM) |
Maximum Junction Temperature (T<sub>J</sub>) | +150°C |

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
## ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $V_{DD} = 2.7\,\text{V to 5.5\,V}$, $V_{SS} = 0\,\text{V}$, $RL = 5\,\text{k}\Omega$, $T_A = -40^\circ\text{C to +125^\circ\text{C}}$. Typical values at $+25^\circ\text{C}$.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Requirements</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage</td>
<td>$V_{DD}$</td>
<td>2.7</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>$V_{REF1:VREF0} = 00$, $V_{OUT}$ is unloaded, volatile DAC Register $= 0x000$</td>
</tr>
<tr>
<td>Input Current</td>
<td>$I_{DD}$</td>
<td>—</td>
<td>210</td>
<td>400</td>
<td>$\mu\text{A}$</td>
<td>$V_{REF1:VREF0} = 11$, $V_{OUT}$ is unloaded, volatile DAC Register $= 0x000$</td>
</tr>
<tr>
<td>Power-Down Current</td>
<td>$I_{DDP}$</td>
<td>—</td>
<td>0.09</td>
<td>2</td>
<td>$\mu\text{A}$</td>
<td>$PD1:PD0 = 0\text{1 (Note 6)}$, $V_{OUT}$ not connected</td>
</tr>
<tr>
<td>Power-On Reset Threshold</td>
<td>$V_{POR}$</td>
<td>—</td>
<td>2.2</td>
<td>—</td>
<td>V</td>
<td>RAM retention voltage, $V_{RAM} &lt; V_{POR}$</td>
</tr>
<tr>
<td>Power-Up Ramp Rate</td>
<td>$V_{RAMP}$</td>
<td>1</td>
<td>—</td>
<td>—</td>
<td>V/S</td>
<td>(Note 1, Note 4)</td>
</tr>
</tbody>
</table>

### DC Accuracy

<table>
<thead>
<tr>
<th>Parameters</th>
<th>$V_{OS}$</th>
<th>$\pm 0.02$</th>
<th>0.75</th>
<th>% of FSR</th>
<th>Code $= 0x000h$</th>
<th>Code $= 0x000h$, $G = 0$</th>
<th>$V_{REF1:VREF0} = 00$, $V_{OUT}$ is unloaded, volatile DAC Register $= 0x000$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset Error Temperature Coefficient</td>
<td>$E_{2S}$</td>
<td>—</td>
<td>0.13</td>
<td>2.0</td>
<td>LSb</td>
<td>MCP4706, Code $= 0x000h$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.52</td>
<td>7.7</td>
<td>LSb</td>
<td>MCP4716, Code $= 0x000h$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>2.05</td>
<td>30.8</td>
<td>LSb</td>
<td>MCP4726, Code $= 0x000h$</td>
<td></td>
</tr>
<tr>
<td>Zero-Scale Error</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full-Scale Error</td>
<td>$E_{FS}$</td>
<td>—</td>
<td>0.3</td>
<td>5.2</td>
<td>LSb</td>
<td>MCP4706, Code $= 0x3FFh$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>1.1</td>
<td>20.5</td>
<td>LSb</td>
<td>MCP4716, Code $= 0x3FFh$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>4.1</td>
<td>82.0</td>
<td>LSb</td>
<td>MCP4726, Code $= 0x3FFh$</td>
<td></td>
</tr>
<tr>
<td>Gain Error (Note 2)</td>
<td>$g_{E}$</td>
<td>-2</td>
<td>-0.1</td>
<td>2</td>
<td>% of FSR</td>
<td>MCP4706, Code $= 0x3FFh$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>-2</td>
<td>-0.1</td>
<td>2</td>
<td>% of FSR</td>
<td>MCP4716, Code $= 0x3FFh$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>-2</td>
<td>-0.1</td>
<td>2</td>
<td>% of FSR</td>
<td>MCP4726, Code $= 0x3FFh$</td>
<td></td>
</tr>
<tr>
<td>Gain Error Drift</td>
<td>$\Delta G/\degree\text{C}$</td>
<td>—</td>
<td>-3</td>
<td>—</td>
<td>ppm/\degree\text{C}</td>
<td>MCP4706</td>
<td></td>
</tr>
<tr>
<td>Resolution</td>
<td>$n$</td>
<td>8</td>
<td>bits</td>
<td></td>
<td></td>
<td>MCP4706</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>bits</td>
<td></td>
<td></td>
<td>MCP4716</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>12</td>
<td>bits</td>
<td></td>
<td></td>
<td>MCP4726</td>
<td></td>
</tr>
<tr>
<td>INL Error (Note 7)</td>
<td>INL</td>
<td>-0.907</td>
<td>±0.125</td>
<td>±0.907</td>
<td>LSb</td>
<td>MCP4706 (codes: 6 to 250)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>-3.625</td>
<td>±0.5</td>
<td>+3.625</td>
<td>LSb</td>
<td>MCP4716 (codes: 25 to 1000)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>-14.5</td>
<td>±2</td>
<td>+14.5</td>
<td>LSb</td>
<td>MCP4726 (codes: 100 to 4000)</td>
<td></td>
</tr>
<tr>
<td>DNL Error (Note 7)</td>
<td>DNL</td>
<td>-0.05</td>
<td>±0.0125</td>
<td>±0.05</td>
<td>LSb</td>
<td>MCP4706 (codes: 6 to 250)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>-0.188</td>
<td>±0.05</td>
<td>+0.188</td>
<td>LSb</td>
<td>MCP4716 (codes: 25 to 1000)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>-0.75</td>
<td>±0.2</td>
<td>+0.75</td>
<td>LSb</td>
<td>MCP4726 (codes: 100 to 4000)</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** This parameter is ensured by design and is not 100% tested.

**Note 2:** This Gain error does not include Offset error. See Section 1.0 “Electrical Characteristics” for more details in plots.

**Note 3:** Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).

**Note 4:** The power-up ramp rate affects on uploading the EEPROM contents to the DAC register. It measures the rise of $V_{DD}$ over time.

**Note 5:** This parameter is ensured by characterization, and not 100% tested.

**Note 6:** $PD1:PD0 = 0\text{1 (Note 6)}$, $V_{OUT}$ not connected.

**Note 7:** $V_{DD} = V_{REF} = 5.5\,\text{V}$. 

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## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Unless otherwise indicated, VDD = 2.7V to 5.5V, VSS = 0V, RL = 5 kΩ from VOUT to GND, CL = 100 pF, TA = -40°C to +125°C. Typical values at +25°C.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Amplifier</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Output Voltage</td>
<td>VOUT(MIN)</td>
<td>—</td>
<td>0.01</td>
<td>—</td>
<td>V</td>
<td>Output Amplifier’s minimum drive</td>
</tr>
<tr>
<td>Maximum Output Voltage</td>
<td>VOUT(MAX)</td>
<td>—</td>
<td>VDD - 0.04</td>
<td>—</td>
<td>V</td>
<td>Output Amplifier’s maximum drive</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>PM</td>
<td>—</td>
<td>66</td>
<td>—</td>
<td>Degree (°)</td>
<td>C_L = 400 pF, R_L = ∞</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>SR</td>
<td>—</td>
<td>0.55</td>
<td>—</td>
<td>V/µs</td>
<td></td>
</tr>
<tr>
<td>Short Circuit Current</td>
<td>ISC</td>
<td>7</td>
<td>15</td>
<td>24</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Settling Time</td>
<td>t_SETTLING</td>
<td>—</td>
<td>6</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>Power-Down Output Disable Time Delay</td>
<td>TPDD</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>µs</td>
<td>Note 3, PD1:PD0 = 00 -&gt; 11, ‘10’, or ‘01’ started from falling edge SCL at end of ACK bit. VOUT = VOUT - 10 mV. VOUT not connected.</td>
</tr>
<tr>
<td>Power-Down Output Enable Time Delay</td>
<td>TPDE</td>
<td>—</td>
<td>10.5</td>
<td>—</td>
<td>µs</td>
<td>Note 3, PD1:PD0 = 11, ‘10’, or ‘01’ -&gt; “00” started from falling edge SCL at end of ACK bit. Volatile DAC Register = FFh, VOUT = 10 mV. VOUT not connected.</td>
</tr>
<tr>
<td>External Reference (VREF) (Note 1)</td>
<td>VREF</td>
<td>0.04</td>
<td>—</td>
<td>VDD - 0.04</td>
<td>V</td>
<td>Buffer mode</td>
</tr>
<tr>
<td>Input Range</td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td></td>
<td>Unbuffered mode</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>RVREF</td>
<td>210</td>
<td>—</td>
<td>VDD</td>
<td>kΩ</td>
<td>Unbuffered mode</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>C_REF</td>
<td>29</td>
<td>—</td>
<td>pF</td>
<td></td>
<td>Unbuffered mode</td>
</tr>
<tr>
<td>-3 dB Bandwidth</td>
<td></td>
<td></td>
<td></td>
<td>86.5</td>
<td>kHz</td>
<td>VREF = 2.048V ± 0.1V, VREF1:VREF0 = 10, G = 0</td>
</tr>
<tr>
<td>Total Harmonic Distortion</td>
<td>THD</td>
<td>-73</td>
<td>—</td>
<td>dB</td>
<td></td>
<td>VREF = 2.048V ± 0.1V, VREF1:VREF0 = 10, G = 0, Frequency = 1 kHz</td>
</tr>
<tr>
<td>Dynamic Performance (Note 1)</td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Major Code Transition Glitch</td>
<td></td>
<td>45</td>
<td>—</td>
<td>nV-s</td>
<td></td>
<td>1 LSB change around major carry (800h to 7FFh)</td>
</tr>
<tr>
<td>Digital Feedthrough</td>
<td></td>
<td></td>
<td>&lt;10</td>
<td>—</td>
<td>nV-s</td>
<td></td>
</tr>
</tbody>
</table>

**Note:**
1. This parameter is ensured by design and is not 100% tested.
2. This Gain error does not include Offset error. See Section 1.0 “Electrical Characteristics” for more details in plots.
3. Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).
4. The power-up ramp rate affects on uploading the EEPROM contents to the DAC register. It measures the rise of VDD over time.
5. This parameter is ensured by characterization, and not 100% tested.
6. The PD1:PD0 = 10, and ‘11’ configurations should have the same current.
7. VDD = VREF = 5.5V.
### ELECTRICAL CHARACTERISTICS (CONTINUED)

#### Digital Interface

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Low Voltage</td>
<td>V_L</td>
<td></td>
<td>0.4</td>
<td></td>
<td>V</td>
<td>I_O_L = 3 mA</td>
</tr>
<tr>
<td>Input High Voltage (SDA and SCL Pins)</td>
<td>V_H</td>
<td>0.7V_D</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Low Voltage (SDA and SCL Pins)</td>
<td>V_L</td>
<td></td>
<td>0.3V_D</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Leakage</td>
<td>I_L</td>
<td></td>
<td>±1</td>
<td></td>
<td>µA</td>
<td>SCL = SDA = V_S or SCL = SDA = V_D</td>
</tr>
<tr>
<td>Pin Capacitance</td>
<td>C_PIN</td>
<td></td>
<td>3</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

#### EEPROM

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEPROM Write Time</td>
<td>T_WRITE</td>
<td>25</td>
<td>50</td>
<td></td>
<td>ms</td>
<td>At +25°C, (Note 1)</td>
</tr>
<tr>
<td>Data Retention</td>
<td></td>
<td>200</td>
<td></td>
<td></td>
<td>Years</td>
<td>At +25°C, (Note 1)</td>
</tr>
<tr>
<td>Endurance</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>Million Cycles</td>
<td>At +25°C, (Note 1)</td>
</tr>
</tbody>
</table>

**Note 1:** This parameter is ensured by design and is not 100% tested.

**Note 2:** This Gain error does not include Offset error. See Section 1.0 “Electrical Characteristics” for more details in plots.

**Note 3:** Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device). The power-up ramp rate affects on uploading the EEPROM contents to the DAC register. It measures the rise of V_DD over time.

**Note 5:** This parameter is ensured by characterization, and not 100% tested.

**Note 6:** The PD1:PD0 = 10, and ‘11’ configurations should have the same current.

**Note 7:** V_DD = V_REF = 5.5V.
1.1  \textit{I}^2\textit{C} Mode Timing Waveforms and Requirements

![Diagram showing power-on and brown-out reset waveforms.](image)

\textbf{FIGURE 1-1:}  Power-On and Brown-Out Reset Waveforms.

![Diagram showing \textit{I}^2\textit{C} power-down command timing.](image)


\textbf{TABLE 1-1:}  \textbf{RESET TIMING}

<table>
<thead>
<tr>
<th>Timing Characteristics</th>
<th>Parameters</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Power-Up Reset Delay</td>
<td>t_{PORD}</td>
<td>60</td>
<td>60</td>
<td>(\mu s)</td>
<td>Monitor ACK bit response to ensure device responds to command.</td>
</tr>
<tr>
<td></td>
<td>Brown-Out Reset Delay</td>
<td>t_{BORD}</td>
<td>1</td>
<td>1</td>
<td>(\mu s)</td>
<td>(V_{DD}) transitions from (V_{DD(MIN)}) (\rightarrow) (V_{POR}) (V_{OUT}) driven to (V_{OUT}) disabled.</td>
</tr>
<tr>
<td></td>
<td>Power-Down Disable Time Delay</td>
<td>(T_{PDD})</td>
<td>2.5</td>
<td>2.5</td>
<td>(\mu s)</td>
<td>(V_{DD} = 5) (V) (PD1:PD0 \rightarrow 00) (from ‘01’, ‘10’, or ‘11’), (PD1:PD0 \rightarrow 00) (from ‘01’, ‘10’, or ‘11’), from falling edge SCL at end of ACK bit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td>(\mu s)</td>
<td>(V_{DD} = 3) (V) (PD1:PD0 \rightarrow 00) (from ‘01’, ‘10’, or ‘11’), (PD1:PD0 \rightarrow 00) (from ‘00’), from falling edge SCL at end of ACK bit.</td>
</tr>
<tr>
<td></td>
<td>Power-Down Enable Time Delay</td>
<td>(T_{PDE})</td>
<td>10.5</td>
<td>10.5</td>
<td>(\mu s)</td>
<td>(PD1:PD0 \rightarrow 01, '10', or '11' (from '00'), from falling edge SCL at end of ACK bit.</td>
</tr>
</tbody>
</table>

\textbf{Notes:}  All parameters apply across the specified operating ranges unless noted. \(V_{DD} = +2.7V\) to 5.5V, 5 k\(\Omega\), 10 k\(\Omega\), 50 k\(\Omega\), 100 k\(\Omega\) devices.

Typical specifications represent values for \(V_{DD} = 5.5V\), \(T_A = +25\degree C\).
**FIGURE 1-3:** $^2$C Bus Start/Stop Bits Timing Waveforms.

**TABLE 1-2:** $^2$C BUS START/STOP BITS REQUIREMENTS

<table>
<thead>
<tr>
<th>$^2$C™ AC Characteristics</th>
<th>Standard Operating Conditions (unless otherwise specified)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Operating Temperature $-40^\circ C \leq TA \leq +125^\circ C$ (Extended)</td>
</tr>
<tr>
<td></td>
<td>Operating Voltage $V_{DD}$ range is described in Electrical Characteristics</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$F_{SCL}$</td>
<td>SCL pin Frequency</td>
<td>Standard mode</td>
<td>0</td>
<td>100 kHz</td>
<td>$C_b = 400 , \text{pF}, 2.7V - 5.5V$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast mode</td>
<td>0</td>
<td>400 kHz</td>
<td>$C_b = 400 , \text{pF}, 2.7V - 5.5V$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed 1.7</td>
<td>0</td>
<td>1.7 MHz</td>
<td>$C_b = 400 , \text{pF}, 4.5V - 5.5V$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed 3.4</td>
<td>0</td>
<td>3.4 MHz</td>
<td>$C_b = 100 , \text{pF}, 4.5V - 5.5V$</td>
<td></td>
</tr>
<tr>
<td>D102</td>
<td>$C_b$</td>
<td>Bus capacitive loading</td>
<td>100 kHz mode</td>
<td>—</td>
<td>400 pF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>—</td>
<td>400 pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.7 MHz mode</td>
<td>—</td>
<td>400 pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.4 MHz mode</td>
<td>—</td>
<td>100 pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>90</td>
<td>TSU:STA</td>
<td>Start condition Setup time</td>
<td>100 kHz mode</td>
<td>4700</td>
<td>— ns</td>
<td>Only relevant for repeated Start condition</td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>600</td>
<td>— ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.7 MHz mode</td>
<td>160</td>
<td>— ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.4 MHz mode</td>
<td>160</td>
<td>— ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>91</td>
<td>THD:STA</td>
<td>Start condition Hold time</td>
<td>100 kHz mode</td>
<td>4000</td>
<td>— ns</td>
<td>After this period, the first clock pulse is generated</td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>600</td>
<td>— ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.7 MHz mode</td>
<td>160</td>
<td>— ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.4 MHz mode</td>
<td>160</td>
<td>— ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>92</td>
<td>TSU:STO</td>
<td>Stop condition Setup time</td>
<td>100 kHz mode</td>
<td>4000</td>
<td>— ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>600</td>
<td>— ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.7 MHz mode</td>
<td>160</td>
<td>— ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.4 MHz mode</td>
<td>160</td>
<td>— ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>93</td>
<td>THD:STO</td>
<td>Stop condition Hold time</td>
<td>100 kHz mode</td>
<td>4000</td>
<td>— ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>600</td>
<td>— ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.7 MHz mode</td>
<td>160</td>
<td>— ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.4 MHz mode</td>
<td>160</td>
<td>— ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>94</td>
<td>$T_{HVCSU}$</td>
<td>HVC to SCL Setup time</td>
<td>25</td>
<td>— uS</td>
<td></td>
<td>High Voltage Commands</td>
</tr>
<tr>
<td>95</td>
<td>$T_{HVCHD}$</td>
<td>SCL to HVC Hold time</td>
<td>25</td>
<td>— uS</td>
<td></td>
<td>High Voltage Commands</td>
</tr>
</tbody>
</table>
### FIGURE 1-4: \( ^{2}C \) Bus Data Timing.

#### TABLE 1-3: \( ^{2}C \) BUS DATA REQUIREMENTS (SLAVE MODE)

<table>
<thead>
<tr>
<th>( ^{2}C ) AC Characteristics</th>
<th>Standard Operating Conditions (unless otherwise specified)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Temperature</td>
<td>(-40^{\circ}C \leq TA \leq +125^{\circ}C) (Extended)</td>
</tr>
<tr>
<td>Operating Voltage V&lt;sub&gt;DD&lt;/sub&gt; range</td>
<td>is described in Electrical Characteristics</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Clock high time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>T_H</td>
<td>100 kHz mode</td>
<td>4000</td>
<td>—</td>
<td>ns</td>
<td>2.7V-5.5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>600</td>
<td>—</td>
<td>ns</td>
<td>2.7V-5.5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.7 MHz mode</td>
<td>120</td>
<td>—</td>
<td>ns</td>
<td>4.5V-5.5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.4 MHz mode</td>
<td>60</td>
<td>—</td>
<td>ns</td>
<td>4.5V-5.5V</td>
</tr>
<tr>
<td>101</td>
<td>T_L</td>
<td>100 kHz mode</td>
<td>4700</td>
<td>—</td>
<td>ns</td>
<td>2.7V-5.5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>1300</td>
<td>—</td>
<td>ns</td>
<td>2.7V-5.5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.7 MHz mode</td>
<td>320</td>
<td>—</td>
<td>ns</td>
<td>4.5V-5.5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.4 MHz mode</td>
<td>160</td>
<td>—</td>
<td>ns</td>
<td>4.5V-5.5V</td>
</tr>
</tbody>
</table>

**Note 1:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**2:** A Fast mode (400 kHz) \( ^{2}C \)™ bus device can be used in a Standard mode (100 kHz) \( ^{2}C \) bus system, but the requirement \( t_{SU:DAT} \geq 250 \) ns must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line.

\[
T_{R_{max}} + t_{SU:DAT} = 1000 + 250 = 1250 \text{ ns (according to the Standard mode } ^{2}C \text{ bus specification) before the SCL line is released.}
\]

**3:** The MCP47X6 device must provide a data hold time to bridge the undefined part between \( V_{IH} \) and \( V_{IL} \) of the falling edge of the SCL signal. This specification is not a part of the \( ^{2}C \) specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

**4:** Use \( C_{0} \) in pF for the calculations.

**5:** Not Tested. This parameter ensured by characterization.

**6:** A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

If this parameter is too short, it can create an unintentional Start or Stop condition to other devices on the \( ^{2}C \) bus line. If this parameter is too long, the Data Input Setup (\( t_{SU:DAT} \)) or Clock Low time (\( T_{LOW} \)) can be affected.

- **Data Input:** This parameter must be longer than \( t_{SP} \).
- **Data Output:** This parameter is characterized, and tested indirectly by testing \( T_{AA} \) parameter.

**7:** Ensured by the \( T_{AA} 3.4 \) MHz specification test.

**8:** The specification is not part of the \( ^{2}C \) specification. \( T_{AA} = T_{HD:DAT} + T_{FSDA} \) (or \( T_{RSDA} \)).
### TABLE 1-3: I²C BUS DATA REQUIREMENTS (SLAVE MODE) (CONTINUED)

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Standard Operating Conditions (unless otherwise specified)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Operating Temperature: -40°C ≤ TA ≤ +125°C (Extended)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Operating Voltage VDD range is described in Electrical Characteristics</td>
</tr>
</tbody>
</table>

#### I²C™ AC Characteristics

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>102A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>102B</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>103A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>103B</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**Note 2:** A Fast mode (400 kHz) I²C™ bus device can be used in a Standard mode (100 kHz) I²C bus system, but the requirement tSU;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line. 

\[ TR_{max} + t_{SU;DAT} = 1000 + 250 = 1250 \text{ ns} \] (according to the Standard mode I²C bus specification) before the SCL line is released.

**Note 3:** The MCP47X6 device must provide a data hold time to bridge the undefined part between VIH and VIL of the falling edge of the SCL signal. This specification is not a part of the I²C specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

**Note 4:** Use \( C_B \) in pF for the calculations.

**Note 5:** Not Tested. This parameter ensured by characterization.

**Note 6:** A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition. If this parameter is too short, it can create an unintentional Start or Stop condition to other devices on the I²C bus line. If this parameter is too long, the Data Input Setup (T_{SU;DAT}) or Clock Low time (T_{LOW}) can be affected.

**Data Input:** This parameter must be longer than t_{SP}.

**Data Output:** This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

**Note 7:** Ensured by the \( T_{AA} \) 3.4 MHz specification test.

**Note 8:** The specification is not part of the I²C specification. \( T_{AA} = T_{HD;DAT} + T_{FSDA} \) (or \( T_{RSDA} \)).
TABLE 1-3:  \( \text{I}^2\text{C™ BUS DATA REQUIREMENTS (SLAVE MODE)} \) (CONTINUED)

<table>
<thead>
<tr>
<th>I(^2\text{C™} ) AC Characteristics</th>
<th>Standard Operating Conditions (unless otherwise specified)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Operating Temperature</strong></td>
<td>(-40^\circ \text{C} \leq T_A \leq +125^\circ \text{C} ) (Extended)</td>
</tr>
<tr>
<td><strong>Operating Voltage</strong> ( V_{DD} )</td>
<td>range is described in Electrical Characteristics</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>106</td>
<td>( T_{HD:DAT} )</td>
<td>Data input hold time</td>
<td>100 kHz mode</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.7 MHz mode</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3.4 MHz mode</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>107</td>
<td>( T_{SU:DAT} )</td>
<td>Data input setup time</td>
<td>100 kHz mode</td>
<td>250</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>100</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.7 MHz mode</td>
<td>10</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3.4 MHz mode</td>
<td>10</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>109</td>
<td>( T_{AA} )</td>
<td>Output valid from clock</td>
<td>100 kHz mode</td>
<td>—</td>
<td>3750</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>—</td>
<td>1200</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.7 MHz mode</td>
<td>—</td>
<td>150</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>310</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3.4 MHz mode</td>
<td>—</td>
<td>150</td>
<td>ns</td>
</tr>
<tr>
<td>110</td>
<td>( T_{BUF} )</td>
<td>Bus free time</td>
<td>100 kHz mode</td>
<td>4700</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>1300</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.7 MHz mode</td>
<td>N/A</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3.4 MHz mode</td>
<td>N/A</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Note 1:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**Note 2:** A Fast mode (400 kHz) \( \text{I}^2\text{C™} \) bus device can be used in a Standard mode (100 kHz) \( \text{I}^2\text{C™} \) bus system, but the requirement \( t_{SU:DAT} \geq 250 \) ns must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line.

\[
T_R + t_{SU:DAT} = 1000 + 250 = 1250 \text{ ns (according to the Standard mode } \text{I}^2\text{C™ bus specification)}
\]

before the SCL line is released.

**Note 3:** The MCP47X6 device must provide a data hold time to bridge the undefined part between \( V_{IH} \) and \( V_{IL} \) of the falling edge of the SCL signal. This specification is not a part of the \( \text{I}^2\text{C™} \) specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

**Note 4:** Use \( C_b \) in pF for the calculations.

**Note 5:** Not Tested. This parameter ensured by characterization.

**Note 6:** A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

If this parameter is too short, it can create an unintentional Start or Stop condition to other devices on the \( \text{I}^2\text{C™} \) bus line. If this parameter is too long, the Data Input Setup (\( T_{SU:DAT} \)) or Clock Low time (\( T_{LOW} \)) can be affected.

**Data Input:** This parameter must be longer than \( t_{SP} \).

**Data Output:** This parameter is characterized, and tested indirectly by testing \( T_{AA} \) parameter.

**Note 7:** Ensured by the \( T_{AA} \) 3.4 MHz specification test.

**Note 8:** The specification is not part of the \( \text{I}^2\text{C™} \) specification. \( T_{AA} = T_{HD:DAT} + T_{FSDA} \) (or \( T_{RSDA} \)).
### TABLE 1-3: I^2C BUS DATA REQUIREMENTS (SLAVE MODE) (CONTINUED)

<table>
<thead>
<tr>
<th>I^2C™ AC Characteristics</th>
<th>Standard Operating Conditions (unless otherwise specified)</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Operating Temperature -40°C ≤ TA ≤ +125°C (Extended)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Operating Voltage V_{DD} range is described in Electrical Characteristics</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>111</td>
<td>T_{SP}</td>
<td>Input filter spike suppression (SDA and SCL)</td>
<td>50 ns</td>
<td>10 ns</td>
<td>Spike suppression</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>100 kHz mode</td>
<td>—</td>
<td>50 ns</td>
<td>NXP Spec states N/A</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>—</td>
<td>50 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.7 MHz mode</td>
<td>—</td>
<td>10 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.4 MHz mode</td>
<td>—</td>
<td>10 ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**Note 2:** A Fast mode (400 kHz) I^2C™ bus device can be used in a Standard mode (100 kHz) I^2C bus system, but the requirement $t_{SU\_DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line.

$$T_{R\_max} + t_{SU\_DAT} = 1000 + 250 = 1250$$ ns (according to the Standard mode I^2C bus specification) before the SCL line is released.

**Note 3:** The MCP47X6 device must provide a data hold time to bridge the undefined part between $V_{IH}$ and $V_{IL}$ of the falling edge of the SCL signal. This specification is not a part of the I^2C specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

**Note 4:** Use $C_b$ in pF for the calculations.

**Note 5:** Not Tested. This parameter ensured by characterization.

**Note 6:** A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

If this parameter is too short, it can create an unintentional Start or Stop condition to other devices on the I^2C bus line. If this parameter is too long, the Data Input Setup ($T_{SU\_DAT}$) or Clock Low time ($T_{LOW}$) can be affected.

**Data Input:** This parameter must be longer than $T_{SP}$

**Data Output:** This parameter is characterized, and tested indirectly by testing $T_{AA}$ parameter.

**Note 7:** Ensured by the $T_{AA}$ 3.4 MHz specification test.

**Note 8:** The specification is not part of the I^2C specification. $T_{AA} = T_{HD\_DAT} + T_{FSDA}$ (or $T_{RSDA}$).
## TEMPERATURE CHARACTERISTICS

### Electrical Specifications: Unless otherwise indicated, $V_{DD} = +2.7V$ to $+5.5V$, $V_{SS} = GND.$

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specified Temperature Range</td>
<td>$T_A$</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>$T_A$</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td>Note 1</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_A$</td>
<td>-65</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

### Thermal Package Resistances

| Thermal Resistance, 6L-SOT-23  | $\theta_{JA}$ | —   | 190    | —   | °C/W  |
| Thermal Resistance, 6L-DFN (2 x 2) | $\theta_{JA}$ | —   | 91     | —   | °C/W  |

**Note 1:** The MCP47X6 devices operate over this extended temperature range, but with reduced performance. Operation in this range must not cause $T_J$ to exceed the Maximum Junction Temperature of +150°C.
2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{RL}$ = Internal, Gain = $x1$, $R_L = 5 \Omega$, $C_L = 100 \mu F$.

**FIGURE 2-1:** INL vs. Code (code = 100 to 4000) and Temperature (MCP4726). $V_{DD} = 5V$, $V_{REF1}:V_{REF0} = 00$.

**FIGURE 2-2:** INL vs. Code (code = 25 to 1000) and Temperature (MCP4716). $V_{DD} = 5V$, $V_{REF1}:V_{REF0} = 00$.

**FIGURE 2-3:** INL vs. Code (code = 6 to 250) and Temperature (MCP4706). $V_{DD} = 5V$, $V_{REF1}:V_{REF0} = 00$.

**FIGURE 2-4:** INL vs. Code (code = 100 to 4000) and Temperature (MCP4726). $V_{DD} = 2.7V$, $V_{REF1}:V_{REF0} = 00$.

**FIGURE 2-5:** INL vs. Code (code = 25 to 1000) and Temperature (MCP4716). $V_{DD} = 2.7V$, $V_{REF1}:V_{REF0} = 00$.

**FIGURE 2-6:** INL vs. Code (code = 6 to 250) and Temperature (MCP4706). $V_{DD} = 2.7V$, $V_{REF1}:V_{REF0} = 00$. 
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{RL} = \text{Internal}$, Gain = $x1$, $R_L = 5 \Omega$, $C_L = 100 \text{ pF}$.

**FIGURE 2-7:** DNL vs. Code (code = 100 to 4000) and Temperature (MCP4726). $V_{DD} = 5V$, $V_{REF1}$:$V_{REF0} = 00$.

**FIGURE 2-8:** DNL vs. Code (code = 25 to 1000) and Temperature (MCP4716). $V_{DD} = 5V$, $V_{REF1}$:$V_{REF0} = 00$.

**FIGURE 2-9:** DNL vs. Code (code = 6 to 250) and Temperature (MCP4706). $V_{DD} = 5V$, $V_{REF1}$:$V_{REF0} = 00$.

**FIGURE 2-10:** DNL vs. Code (code = 100 to 4000) and Temperature (MCP4726). $V_{DD} = 2.7V$, $V_{REF1}$:$V_{REF0} = 00$.

**FIGURE 2-11:** DNL vs. Code (code = 25 to 1000) and Temperature (MCP4716). $V_{DD} = 2.7V$, $V_{REF1}$:$V_{REF0} = 00$.

**FIGURE 2-12:** DNL vs. Code (code = 6 to 250) and Temperature (MCP4706). $V_{DD} = 2.7V$, $V_{REF1}$:$V_{REF0} = 00$. 

Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{RL} =$ Internal, Gain = x1, $R_L = 5 \, k\Omega$, $C_L = 100 \, pF$.

**FIGURE 2-13:** Zero-Scale Error (ZSE) vs. $V_{DD}$ and Temperature (MCP4726). $V_{REF1}:V_{REF0} = 00$.

**FIGURE 2-14:** Zero-Scale Error (ZSE) vs. $V_{DD}$ and Temperature (MCP4716). $V_{REF1}:V_{REF0} = 00$.

**FIGURE 2-15:** Zero-Scale Error (ZSE) vs. $V_{DD}$ and Temperature (MCP4706). $V_{REF1}:V_{REF0} = 00$.

**FIGURE 2-16:** Full-Scale Error (FSE) vs. $V_{DD}$ and Temperature (MCP4726). $V_{REF1}:V_{REF0} = 00$.

**FIGURE 2-17:** Full-Scale Error (FSE) vs. $V_{DD}$ and Temperature (MCP4716). $V_{REF1}:V_{REF0} = 00$.

**FIGURE 2-18:** Full-Scale Error (FSE) vs. $V_{DD}$ and Temperature (MCP4706). $V_{REF1}:V_{REF0} = 00$. 
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{RL} =$ Internal, Gain = $x1$, $R_L = 5 \, k\Omega$, $C_L = 100 \, pF$.

**FIGURE 2-19:** INL vs. Code (code = 100 to 4000) and Temperature (MCP4726). $V_{DD} = 5V$, $V_{REF1}$:$V_{REF0} = 10$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-20:** INL vs. Code (code = 25 to 1000) and Temperature (MCP4716). $V_{DD} = 5V$, $V_{REF1}$:$V_{REF0} = 10$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-21:** INL vs. Code (code = 6 to 250) and Temperature (MCP4706). $V_{DD} = 5V$, $V_{REF1}$:$V_{REF0} = 10$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-22:** INL vs. Code (code = 100 to 4000) and Temperature (MCP4726). $V_{DD} = 2.7V$, $V_{REF1}$:$V_{REF0} = 10$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-23:** INL vs. Code (code = 25 to 1000) and Temperature (MCP4716). $V_{DD} = 2.7V$, $V_{REF1}$:$V_{REF0} = 10$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-24:** INL vs. Code (code = 6 to 250) and Temperature (MCP4706). $V_{DD} = 2.7V$, $V_{REF1}$:$V_{REF0} = 10$, $G = 0$, $V_{REF} = V_{DD}$.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{RL} = \text{Internal}$, Gain = $x1$, $R_L = 5\, k\Omega$, $C_L = 100\, pF$.

**FIGURE 2-25:** DNL vs. Code (code = 100 to 4000) and Temperature (MCP4726).

$V_{DD} = 5V$, $V_{REF1:VREF0} = 10$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-26:** DNL vs. Code (code = 25 to 1000) and Temperature (MCP4716).

$V_{DD} = 5V$, $V_{REF1:VREF0} = 10$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-27:** DNL vs. Code (code = 6 to 250) and Temperature (MCP4706).

$V_{DD} = 5V$, $V_{REF1:VREF0} = 10$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-28:** DNL vs. Code (code = 100 to 4000) and Temperature (MCP4726).

$V_{DD} = 2.7V$, $V_{REF1:VREF0} = 10$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-29:** DNL vs. Code (code = 25 to 1000) and Temperature (MCP4716).

$V_{DD} = 2.7V$, $V_{REF1:VREF0} = 10$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-30:** DNL vs. Code (code = 6 to 250) and Temperature (MCP4706).

$V_{DD} = 2.7V$, $V_{REF1:VREF0} = 10$, $G = 0$, $V_{REF} = V_{DD}$.
Note: Unless otherwise indicated, \( T_A = +25^\circ C \), \( V_{DD} = 5V \), \( V_{SS} = 0V \), \( V_{RL} \) = Internal, Gain = x1, \( R_L = 5 \, k\Omega \), \( C_L = 100 \, pF \).

**FIGURE 2-31:** Zero-Scale Error (ZSE) vs. Temperature (MCP4726).
\( V_{DD} = 5V \), \( V_{REF1}:V_{REF0} = 1.0 \), \( G = 0 \), \( V_{REF} = V_{DD} \).

**FIGURE 2-32:** Zero-Scale Error (ZSE) vs. Temperature (MCP4716).
\( V_{DD} = 5V \), \( V_{REF1}:V_{REF0} = 1.0 \), \( G = 0 \), \( V_{REF} = V_{DD} \).

**FIGURE 2-33:** Zero-Scale Error (ZSE) vs. Temperature (MCP4706).
\( V_{DD} = 5V \), \( V_{REF1}:V_{REF0} = 1.0 \), \( G = 0 \), \( V_{REF} = V_{DD} \).

**FIGURE 2-34:** Full-Scale Error (FSE) vs. Temperature (MCP4726).
\( V_{DD} = 2.7V \), \( V_{REF1}:V_{REF0} = 1.0 \), \( G = 0 \), \( V_{REF} = V_{DD} \).

**FIGURE 2-35:** Full-Scale Error (FSE) vs. Temperature (MCP4716).
\( V_{DD} = 2.7V \), \( V_{REF1}:V_{REF0} = 1.0 \), \( G = 0 \), \( V_{REF} = V_{DD} \).

**FIGURE 2-36:** Full-Scale Error (FSE) vs. Temperature (MCP4706).
\( V_{DD} = 2.7V \), \( V_{REF1}:V_{REF0} = 1.0 \), \( G = 0 \), \( V_{REF} = V_{DD} \).
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{RL} =$ Internal, Gain = x1, $R_L = 5 \, k\Omega$, $C_L = 100 \, pF$.

**FIGURE 2-37:** INL vs. Code (code = 100 to 4000) and Temperature (MCP4726).
$V_{DD} = 5V$, $V_{REF1}:V_{REF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-38:** INL vs. Code (code = 25 to 1000) and Temperature (MCP4716).
$V_{DD} = 5V$, $V_{REF1}:V_{REF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-39:** INL vs. Code (code = 6 to 250) and Temperature (MCP4706).
$V_{DD} = 5V$, $V_{REF1}:V_{REF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-40:** INL vs. Code (code = 100 to 4000) and Temperature (MCP4726).
$V_{DD} = 2.7V$, $V_{REF1}:V_{REF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-41:** INL vs. Code (code = 25 to 1000) and Temperature (MCP4716).
$V_{DD} = 2.7V$, $V_{REF1}:V_{REF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-42:** INL vs. Code (code = 6 to 250) and Temperature (MCP4706).
$V_{DD} = 2.7V$, $V_{REF1}:V_{REF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{RL} = \text{Internal}$, Gain = x1, $R_L = 5 \, k\Omega$, $C_L = 100 \, pF$.

**FIGURE 2-43:** DNL vs. Code (code = 100 to 4000) and Temperature (MCP4726).
$V_{DD} = 5V$, $V_{REF1:VREF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-44:** DNL vs. Code (code = 25 to 1000) and Temperature (MCP4716).
$V_{DD} = 5V$, $V_{REF1:VREF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-45:** DNL vs. Code (code = 6 to 250) and Temperature (MCP4706).
$V_{DD} = 5V$, $V_{REF1:VREF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-46:** DNL vs. Code (code = 100 to 4000) and Temperature (MCP4726).
$V_{DD} = 2.7V$, $V_{REF1:VREF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-47:** DNL vs. Code (code = 25 to 1000) and Temperature (MCP4716).
$V_{DD} = 2.7V$, $V_{REF1:VREF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-48:** DNL vs. Code (code = 6 to 250) and Temperature (MCP4706).
$V_{DD} = 2.7V$, $V_{REF1:VREF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$. 
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{RL}$ = Internal, Gain = x1, $R_L = 5 \, k\Omega$, $C_L = 100 \, pF$. 

**FIGURE 2-49:** Zero-Scale Error (ZSE) vs. Temperature (MCP4726). $V_{DD} = 5V$, $V_{REF1}:V_{REF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.  

**FIGURE 2-50:** Zero-Scale Error (ZSE) vs. Temperature (MCP4716). $V_{DD} = 5V$, $V_{REF1}:V_{REF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.  

**FIGURE 2-51:** Zero-Scale Error (ZSE) vs. Temperature (MCP4706). $V_{DD} = 5V$, $V_{REF1}:V_{REF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.  

**FIGURE 2-52:** Full-Scale Error (FSE) vs. Temperature (MCP4726). $V_{DD} = 2.7V$, $V_{REF1}:V_{REF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.  

**FIGURE 2-53:** Full-Scale Error (FSE) vs. Temperature (MCP4716). $V_{DD} = 2.7V$, $V_{REF1}:V_{REF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.  

**FIGURE 2-54:** Full-Scale Error (FSE) vs. Temperature (MCP4706). $V_{DD} = 2.7V$, $V_{REF1}:V_{REF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{RL} = \text{Internal}$, Gain = $x1$, $R_L = 5\, k\Omega$, $C_L = 100\, pF$. 

**FIGURE 2-55:** INL vs. Code (code = 100 to 4000) and $V_{DD}$ (2.7V, 5V, 5.5V) (MCP4726). $V_{REF}:V_{REF0} = 10$, $G = 1$, $V_{REF} = V_{DD}/2$, Temp = $+25^\circ C$. 

**FIGURE 2-56:** INL vs. Code (code = 25 to 1000) and $V_{DD}$ (2.7V, 5V, 5.5V) (MCP4716). $V_{REF}:V_{REF0} = 10$, $G = 1$, $V_{REF} = V_{DD}/2$, Temp = $+25^\circ C$. 

**FIGURE 2-57:** INL vs. Code (code = 6 to 250) and $V_{DD}$ (2.7V, 5V, 5.5V) (MCP4706). $V_{REF}:V_{REF0} = 10$, $G = 1$, $V_{REF} = V_{DD}/2$, Temp = $+25^\circ C$. 

**FIGURE 2-58:** DNL vs. Code (code = 100 to 4000) and $V_{DD}$ (2.7V, 5V, 5.5V) (MCP4726). $V_{REF}:V_{REF0} = 10$, $G = 1$, $V_{REF} = V_{DD}/2$, Temp = $+25^\circ C$. 

**FIGURE 2-59:** DNL vs. Code (code = 25 to 1000) and $V_{DD}$ (2.7V, 5V, 5.5V) (MCP4716). $V_{REF}:V_{REF0} = 10$, $G = 1$, $V_{REF} = V_{DD}/2$, Temp = $+25^\circ C$. 

**FIGURE 2-60:** DNL vs. Code (code = 6 to 250) and $V_{DD}$ (2.7V, 5V, 5.5V) (MCP4706). $V_{REF}:V_{REF0} = 10$, $G = 1$, $V_{REF} = V_{DD}/2$, Temp = $+25^\circ C$. 

Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{RL}$ = Internal, Gain = x1, $R_L = 5 \, k\Omega$, $C_L = 100 \, pF$. 

**FIGURE 2-61**: INL vs. Code (code = 100 to 4000) and $V_{DD}$ (2.7V, 5V, 5.5V) (MCP4726).
$V_{REF1}:V_{REF0} = 1:1$, $G = 1$, $V_{REF} = V_{DD}/2$.
Temp = +25°C.

**FIGURE 2-62**: INL vs. Code (code = 25 to 1000) and $V_{DD}$ (2.7V, 5V, 5.5V) (MCP4716).
$V_{REF1}:V_{REF0} = 1:1$, $G = 1$, $V_{REF} = V_{DD}/2$.
Temp = +25°C.

**FIGURE 2-63**: INL vs. Code (code = 6 to 250) and $V_{DD}$ (2.7V, 5V, 5.5V) (MCP4706).
$V_{REF1}:V_{REF0} = 1:1$, $G = 1$, $V_{REF} = V_{DD}/2$.
Temp = +25°C.

**FIGURE 2-64**: DNL vs. Code (code = 100 to 4000) and $V_{DD}$ (2.7V, 5V, 5.5V) (MCP4726).
$V_{REF1}:V_{REF0} = 1:1$, $G = 1$, $V_{REF} = V_{DD}/2$.
Temp = +25°C.

**FIGURE 2-65**: DNL vs. Code (code = 25 to 1000) and $V_{DD}$ (2.7V, 5V, 5.5V) (MCP4716).
$V_{REF1}:V_{REF0} = 1:1$, $G = 1$, $V_{REF} = V_{DD}/2$.
Temp = +25°C.

**FIGURE 2-66**: DNL vs. Code (code = 6 to 250) and $V_{DD}$ (2.7V, 5V, 5.5V) (MCP4706).
$V_{REF1}:V_{REF0} = 1:1$, $G = 1$, $V_{REF} = V_{DD}/2$.
Temp = +25°C.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{RL} = \text{Internal}$, Gain = x1, $R_L = 5\Omega$, $C_L = 100\ pF$.

**FIGURE 2-67:** INL vs. Code (code = 100 to 4000) and $V_{REF}$ (MCP4726).
$V_{DD} = 5V$, $V_{REF1}:V_{REF0} = 1:0$, $G = 0$,
$V_{REF} = 1V, 2V, 3V, 4V, \text{ and } 5V$, Temp = +25°C.

**FIGURE 2-68:** INL vs. Code (code = 25 to 1000) and $V_{REF}$ (MCP4716).
$V_{DD} = 5V$, $V_{REF1}:V_{REF0} = 1:0$, $G = 0$,
$V_{REF} = 1V, 2V, 3V, 4V, \text{ and } 5V$, Temp = +25°C.

**FIGURE 2-69:** INL vs. Code (code = 6 to 250) and $V_{REF}$ (MCP4706).
$V_{DD} = 5V$, $V_{REF1}:V_{REF0} = 1:0$, $G = 0$,
$V_{REF} = 1V, 2V, 3V, 4V, \text{ and } 5V$, Temp = +25°C.

**FIGURE 2-70:** DNL vs. Code (code = 100 to 4000) and $V_{REF}$ (MCP4726).
$V_{DD} = 5V$, $V_{REF1}:V_{REF0} = 1:0$, $G = 0$,
$V_{REF} = 1V, 2V, 3V, 4V, \text{ and } 5V$, Temp = +25°C.

**FIGURE 2-71:** DNL vs. Code (code = 25 to 1000) and $V_{REF}$ (MCP4716).
$V_{DD} = 5V$, $V_{REF1}:V_{REF0} = 1:0$, $G = 0$,
$V_{REF} = 1V, 2V, 3V, 4V, \text{ and } 5V$, Temp = +25°C.

**FIGURE 2-72:** DNL vs. Code (code = 6 to 250) and $V_{REF}$ (MCP4706).
$V_{DD} = 5V$, $V_{REF1}:V_{REF0} = 1:0$, $G = 0$,
$V_{REF} = 1V, 2V, 3V, 4V, \text{ and } 5V$, Temp = +25°C.
**MCP4706/4716/4726**

**Note:** Unless otherwise indicated, \( T_A = +25^\circ C \), \( V_{DD} = 5V \), \( V_{SS} = 0V \), \( V_{RL} = \) Internal, Gain = \( x1 \), \( R_L = 5 \, k\Omega \), \( C_L = 100 \, pF \).

**FIGURE 2-73:** INL vs. Code (code = 100 to 4000) and \( V_{REF} \) (MCP4726).

\( V_{DD} = 5V \), \( V_{REF1}:V_{REF0} = 1:1 \), \( G = 0 \),
\( V_{REF} = 1V, 2V, 3V, 4V, \) and \( 5V \), Temp = +25°C.

**FIGURE 2-74:** INL vs. Code (code = 25 to 1000) and \( V_{REF} \) (MCP4716).

\( V_{DD} = 5V \), \( V_{REF1}:V_{REF0} = 1:1 \), \( G = 0 \),
\( V_{REF} = 1V, 2V, 3V, 4V, \) and \( 5V \), Temp = +25°C.

**FIGURE 2-75:** INL vs. Code (code = 6 to 250) and \( V_{REF} \) (MCP4706).

\( V_{DD} = 5V \), \( V_{REF1}:V_{REF0} = 1:1 \), \( G = 0 \),
\( V_{REF} = 1V, 2V, 3V, 4V, \) and \( 5V \), Temp = +25°C.

**FIGURE 2-76:** DNL vs. Code (code = 100 to 4000) and \( V_{REF} \) (MCP4726).

\( V_{DD} = 5V \), \( V_{REF1}:V_{REF0} = 1:1 \), \( G = 0 \),
\( V_{REF} = 1V, 2V, 3V, 4V, \) and \( 5V \), Temp = +25°C.

**FIGURE 2-77:** DNL vs. Code (code = 25 to 1000) and \( V_{REF} \) (MCP4716).

\( V_{DD} = 5V \), \( V_{REF1}:V_{REF0} = 1:1 \), \( G = 0 \),
\( V_{REF} = 1V, 2V, 3V, 4V, \) and \( 5V \), Temp = +25°C.

**FIGURE 2-78:** DNL vs. Code (code = 6 to 250) and \( V_{REF} \) (MCP4706).

\( V_{DD} = 5V \), \( V_{REF1}:V_{REF0} = 1:1 \), \( G = 0 \),
\( V_{REF} = 1V, 2V, 3V, 4V, \) and \( 5V \), Temp = +25°C.
Note: Unless otherwise indicated, $T_A = +25\,^\circ\text{C}$, $V_{\text{DD}} = 5\,\text{V}$, $V_{\text{SS}} = 0\,\text{V}$, $V_{\text{RL}} = \text{Internal}$, Gain = $x1$, $R_L = 5\,\text{k}\Omega$, $C_L = 100\,\text{pF}$.

FIGURE 2-79: Output Error vs. Temperature (MCP4726). $V_{\text{DD}} = 2.7\,\text{V}$ and $5\,\text{V}$, $V_{\text{REF}}:V_{\text{REF}0} = 00$, Code = 4000.

FIGURE 2-80: Output Error vs. Temperature (MCP4716). $V_{\text{DD}} = 2.7\,\text{V}$ and $5\,\text{V}$, $V_{\text{REF}}:V_{\text{REF}0} = 00$, Code = 1000.

FIGURE 2-81: Output Error vs. Temperature (MCP4706). $V_{\text{DD}} = 2.7\,\text{V}$ and $5\,\text{V}$, $V_{\text{REF}}:V_{\text{REF}0} = 00$, Code = 250.

FIGURE 2-82: Output Error vs. Temperature (MCP4726). $V_{\text{DD}} = 2.7\,\text{V}$ and $5\,\text{V}$, $V_{\text{REF}}:V_{\text{REF}0} = 10$, $G = 0$, $V_{\text{REF}} = V_{{\text{DD}}}$, Code = 4000.

FIGURE 2-83: Output Error vs. Temperature (MCP4716). $V_{\text{DD}} = 2.7\,\text{V}$ and $5\,\text{V}$, $V_{\text{REF}}:V_{\text{REF}0} = 10$, $G = 0$, $V_{\text{REF}} = V_{{\text{DD}}}$, Code = 1000.

FIGURE 2-84: Output Error vs. Temperature (MCP4706). $V_{\text{DD}} = 2.7\,\text{V}$ and $5\,\text{V}$, $V_{\text{REF}}:V_{\text{REF}0} = 10$, $G = 0$, $V_{\text{REF}} = V_{{\text{DD}}}$, Code = 250.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{RL} = \text{Internal}$, $\text{Gain} = x1$, $R_L = 5 \, k\Omega$, $C_L = 100 \, \text{pF}$.

**FIGURE 2-85:** Output Error vs. Temperature (MCP4726). $V_{DD} = 2.7V$ and $5V$, $V_{REF1}:V_{REF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$, Code = 4000.

**FIGURE 2-86:** Output Error vs. Temperature (MCP4716). $V_{DD} = 2.7V$ and $5V$, $V_{REF1}:V_{REF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$, Code = 1000.

**FIGURE 2-87:** Output Error vs. Temperature (MCP4706). $V_{DD} = 2.7V$ and $5V$, $V_{REF1}:V_{REF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$, Code = 250.
**Note:** Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{RL} = $ Internal, Gain = x1, $R_L = 5 \, k\Omega$, $C_L = 100 \, pF$.

**FIGURE 2-88:** $I_{DD}$ vs. Temperature. $V_{DD} = 2.7V$ and $5V$, $V_{REF1}:V_{REF0} = 00$.

**FIGURE 2-89:** $I_{DD}$ vs. Temperature. $V_{DD} = 2.7V$ and $5V$, $V_{REF1}:V_{REF0} = 10$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-90:** $I_{DD}$ vs. Temperature. $V_{DD} = 2.7V$ and $5V$, $V_{REF1}:V_{REF0} = 11$, $G = 0$, $V_{REF} = V_{DD}$.

**FIGURE 2-91:** Power-down Current vs. Temperature. $V_{DD} = 2.7V$, $3.3V$, $4.5V$, $5.0V$ and $5.5V$, $PD1:PD0 = 11$. 
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{RL} = \text{Internal}$, Gain = $x1$, $R_L = 5 \, k\Omega$, $C_L = 100 \, pF$.

**FIGURE 2-92:** $V_{IH}$ Threshold of SDA/SCL Inputs vs. Temperature and $V_{DD}$.

**FIGURE 2-93:** $V_{IL}$ Threshold of SDA/SCL Inputs vs. Temperature and $V_{DD}$.

**FIGURE 2-94:** $V_{OUT}$ vs. Resistive Load. $V_{DD} = 5.0V$.

**FIGURE 2-95:** $V_{OUT}$ vs. Source/Sink Current. $V_{DD} = 5.0V$. 
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{REF} =$ Internal, Gain = $x1$, $R_L = 5 k\Omega$, $C_L = 100$ pF.

**FIGURE 2-96:** Full-Scale Settling Time (000h to FFFh) (*MCP4726*).

**FIGURE 2-97:** Full-Scale Settling Time (FFFh to 000h) (*MCP4726*).

**FIGURE 2-98:** Half-Scale Settling Time (400h to C00h) (*MCP4726*).

**FIGURE 2-99:** Half-Scale Settling Time (C00h to 400h) (*MCP4726*).

**FIGURE 2-100:** Exiting Power-Down Mode (*MCP4726, Volatile DAC Register = FFFh*).
## 3.0 PIN DESCRIPTIONS

An overview of the pin functions are described in Section 3.1 “Analog Output Voltage Pin (VOUT)” through Section 3.7 “Exposed Pad (EP)”. The descriptions of the pins are listed in Table 3-1.

### TABLE 3-1: MCP47X6 PINOUT DESCRIPTION

<table>
<thead>
<tr>
<th>SOT-23</th>
<th>DFN</th>
<th>Symbol</th>
<th>I/O</th>
<th>Buffer Type</th>
<th>Standard Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>6L</td>
<td>6L</td>
<td>V\textsubscript{OUT}</td>
<td>A</td>
<td>Analog</td>
<td>Buffered analog voltage output pin</td>
</tr>
<tr>
<td>2</td>
<td>5</td>
<td>V\textsubscript{SS}</td>
<td>—</td>
<td>P</td>
<td>Ground reference pin for all circuitries on the device</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>V\textsubscript{DD}</td>
<td>—</td>
<td>P</td>
<td>Supply Voltage Pin</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
<td>SDA</td>
<td>I/O</td>
<td>ST</td>
<td>I\textsuperscript{2}C™ Serial Data Pin</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>SCL</td>
<td>I</td>
<td>ST</td>
<td>I\textsuperscript{2}C Serial Clock Pin</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>V\textsubscript{REF}</td>
<td>A</td>
<td>Analog</td>
<td>Voltage Reference Input Pin</td>
</tr>
<tr>
<td>—</td>
<td>7</td>
<td>EP</td>
<td>—</td>
<td>—</td>
<td>Exposed Pad (Note 1)</td>
</tr>
</tbody>
</table>

Legend:  
A = Analog pins  
O = Digital output  
I = Digital input (high Z)  
I/O = Input / Output  
P = Power

**Note 1:** The DFN package has a contact on the bottom of the package. This contact is conductively connected to the die substrate, and therefore should be unconnected or connected to the same ground as the device’s V\textsubscript{SS} pin.
3.1 Analog Output Voltage Pin (VOUT)

VOUT is the DAC analog output pin. The DAC output has an output amplifier. VOUT can swing from approximately 0V to approximately VDD. The full-scale range of the DAC output is from VSS to G * VRL, where G is the gain selection option (1x or 2x).

In Normal mode, the DC impedance of the output pin is about 1Ω. In Power-Down mode, the output pin is internally connected to a known pull-down resistor of 1kΩ, 125kΩ, or 640kΩ. The power-down selection bits settings are shown in Table 4-2.

3.2 Positive Power Supply Input (VDD)

VDD is the positive supply voltage input pin. The input supply voltage is relative to VSS.

The power supply at the VDD pin should be as clean as possible for a good DAC performance. It is recommended to use an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate high-frequency noise present in application boards.

3.3 Ground (VSS)

The VSS pin is the device ground reference.

The user must connect the VSS pin to a ground plane through a low-impedance connection. If an analog ground path is available in the application Printed Circuit Board (PCB), it is highly recommended that the VSS pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.4 Serial Data Pin (SDA)

SDA is the serial data pin of the I²C interface. The SDA pin is used to write or read the DAC registers and Configuration bits. The SDA pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the VDD line to the SDA pin. Except for Start and Stop conditions, the data on the SDA pin must be stable during the high period of the clock. The high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. Refer to Section 5.0 “I²C Serial Interface” for more details of I²C serial interface communication.

3.5 Serial Clock Pin (SCL)

SCL is the serial clock pin of the I²C interface. The MCP47X6 devices act only as a slave and the SCL pin accepts only external serial clocks. The input data from the master device is shifted into the SDA pin on the rising edges of the SCL clock and output from the device occurs at the falling edges of the SCL clock. The SCL pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the VDD line to the SCL pin. Refer to Section 5.0 “I²C Serial Interface” for more details about I²C serial interface communication.

3.6 Voltage Reference Pin (VREF)

This pin is used for the external voltage reference input. The user can select VDD voltage or the VREF pin voltage as the reference resistor ladder’s voltage reference.

When the VREF pin signal is selected, there is an option for this voltage to be buffered or unbuffered. This is offered in cases where the reference voltage does not have the current capability not to drop its voltage when connected to the internal resistor ladder circuit.

When the VDD is selected as reference voltage, this pin is disconnected from the internal circuit.

See Section 4.2 “DAC’s (Resistor Ladder) Reference Voltage” and Table 4-4 for more details on the Configuration bits.

3.7 Exposed Pad (EP)

This pad is conductively connected to the device’s substrate. This pad should be tied to the same potential as the VSS pin (or left unconnected). This pad could be used to assist as a heat sink for the device when connected to a PCB heat sink.
4.0 GENERAL DESCRIPTION

The MCP4706, MCP4716, and MCP4726 devices are single channel voltage output 8-bit, 10-bit, and 12-bit DAC devices with nonvolatile memory (EEPROM) and an I2C serial interface. This family will be referred to as MCP47X6.

The devices use a resistor ladder architecture. The resistor ladder DAC is driven from a software selectable voltage reference source. The source can be either the device's internal VDD or the external VREF pin voltage.

The DAC output is buffered with a low power and precision output amplifier (op amp). This output amplifier provides a rail-to-rail output with low offset voltage and low noise. The gain of the output buffer is software configurable.

This device also has user programmable nonvolatile memory (EEPROM), which allows the user to save the desired POR/BOR value of the DAC register and device Configuration bits.

The devices use a two-wire I2C serial communication interface and operate with a single supply voltage from 2.7V to 5.5V.

4.1 Power-On Reset/Brown-Out Reset (POR/BOR)

The internal Power-on Reset (POR)/Brown-out Reset (BOR) circuit monitors the power supply voltage (VDD) during operation. This circuit ensures correct device start-up at system power-up and power-down events. VREF is the RAM retention voltage and is always lower than the POR trip point voltage.

POR occurs as the voltage is rising (typically from 0V), while BOR occurs as the voltage is falling (typically from VDD(MIN) or higher).

When the rising VDD voltage crosses the VPOR trip point, the following occurs:

- Nonvolatile DAC register value latched into volatile DAC register
- Nonvolatile Configuration bit values latched into volatile Configuration bits
- POR Status bit is set ("1")
- The Reset delay timer starts; when timer times out (tPORD), the I2C interface is operational.

The analog output (VOUT) state will be determined by the state of the volatile Configuration bits and the DAC register. This is called a POR Reset (event).

When the falling VDD voltage crosses the VPOR trip point, the following occurs:

- Device is forced into a power-down state (PD1:PD0 = 11). Analog circuitry is turned off.
- Volatile DAC register is forced to 000h
- Volatile Configuration bits VREF1, VREF0 and G are forced to '0'

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

<table>
<thead>
<tr>
<th>VDD(MIN)</th>
<th>VPOR</th>
<th>VRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device in unknown state</td>
<td>Device in POR state</td>
<td>POR Reset forced active</td>
</tr>
<tr>
<td>POR starts Reset Delay Timer. When timer times out, I2C interface can operate (if VDD &gt;= VDD(MIN))</td>
<td>Normal Operation</td>
<td>Volatile memory retains data value</td>
</tr>
<tr>
<td>Below minimum operating voltage</td>
<td>Device in power down state</td>
<td>Volatile memory becomes corrupted</td>
</tr>
<tr>
<td>BOR Reset, volatile DAC Register = 000h</td>
<td>VREF1:VREF0 = 00</td>
<td>volatile G = 0</td>
</tr>
<tr>
<td></td>
<td>volatile PD1:PD0 = 11</td>
<td></td>
</tr>
</tbody>
</table>

*Figure 4-1: Power-on Reset Operation.*
4.2 DAC’s (Resistor Ladder) Reference Voltage

The device can be configured to use one of three voltage sources for the resistor ladder’s reference voltage (VRL) (see Figure 4-2). These are:
1. VDD pin voltage
2. VREF pin voltage internally buffered
3. VREF pin voltage unbuffered

The selection of the voltage is specified with the volatile VREF1:VREF0 Configuration bits (see Table 4-4). There are nonvolatile and volatile VREF1:VREF0 Configuration bits. On a POR/BOR event, the state of the nonvolatile VREF1:VREF0 Configuration bits are latched into the volatile VREF1:VREF0 Configuration bits.

When the user selects the VDD as reference, the VREF pin voltage is not connected to the resistor ladder.

If the VREF pin is selected, then select between the Buffered or Unbuffered mode.

In Unbuffered mode, the VREF pin voltage may be from VSS to VDD.

**Note:** In Unbuffered mode, the voltage source should have a low output impedance. If the voltage source has a high output impedance, then the voltage on the VREF’s pin would be lower than expected. The resistor ladder has a typical impedance of 210 kΩ and a typical capacitance of 29 pF.

In Buffered mode, the VREF pin voltage may be from 0.01V to VDD-0.04V. The input buffer (amplifier) provides low offset voltage, low noise, and a very high input impedance, with only minor limitations on the input range and frequency response.

**Note:** Any variation or noises on the reference source can directly affect the DAC output. The reference voltage needs to be as clean as possible for accurate DAC performance.

![Resistor Ladder Reference Voltage Selection Block Diagram](image)

**FIGURE 4-2:** Resistor Ladder Reference Voltage Selection Block Diagram.

4.3 Resistor Ladder

The resistor ladder is a digital potentiometer with the B Terminal internally grounded and the A terminal connected to the selected reference voltage (see Figure 4-3). The volatile DAC register controls the wiper position. The wiper voltage (VW) is proportional to the DAC register value divided by the number of resistor elements (R_S) in the ladder (256, 1024, or 4096) related to the VRL voltage.

**Note:** The maximum wiper position is 2^n - 1, while the number of resistors in the resistor ladder is 2^n. This means that when the DAC register is at full scale, there is one resistor element (R_S) between the wiper and the VRL voltage.

The resistor ladder (RRL) has a typical impedance of approximately 210 kΩ. This resistor ladder resistance (RRL) may vary from device to device up to ±20%. Since this is a voltage divider configuration, the actual RRL resistance does not effect the output given a fixed voltage at VRL.

If the unbuffered VREF pin is used as the VRL voltage source, this voltage source should have a low output impedance.

When the DAC is powered down, the resistor ladder is disconnected from the selected reference voltage.

![Resistor Ladder](image)

**FIGURE 4-3:** Resistor Ladder.

\[
V_W = \frac{\text{DAC Register Value}}{\# \text{Resistors in Resistor Ladder}} \times V_{RL}
\]

Where:
- \# Resistors in Resistor Ladder = 256 (MCP4706)
- 1024 (MCP4716)
- 4096 (MCP4726)
4.4 Output Buffer/VOUT Operation

The DAC output is buffered with a low power and precision output amplifier (op amp). Figure 4-4 shows a block diagram.

This amplifier provides a rail-to-rail output with low offset voltage and low noise. The user can select the output gain of the output amplifier. Gain options are:

a) Gain of 1, with either V_DD or V_REF pin used as reference voltage

b) Gain of 2, only when V_REF pin is used as reference voltage. The V_REF pin voltage should be limited to V_DD/2.

The amplifier’s output can drive the resistive and high capacitive loads without oscillation. The amplifier provides a maximum load current which is enough for most programmable voltage reference applications. Refer to Section 1.0 “Electrical Characteristics” for the specifications of the output amplifier.

In any of the three Power-Down modes, the op amp is powered down and its output becomes a high-impedance to the VOUT pin.

Note: The load resistance must stay higher than 5 kΩ for the stable and expected analog output to meet electrical specifications.

4.4.1 PROGRAMMABLE GAIN

The amplifier’s gain is controlled by the Gain (G) Configuration bit (See Table 4-4) and the VRL reference selection. When the VRL reference selection is the device’s V_DD voltage, the G bit is ignored and a gain of 1 is used. The volatile G bit value can be modified by:

• POR event
• BOR event
• I2C Write commands
• I2C General Call Reset command

4.4.2 OUTPUT VOLTAGE

The volatile DAC register’s value controls the analog VOUT voltage, along with the device’s five Configuration bits. The volatile DAC register’s value is unsigned binary.

The formula for the output voltage is given in Equation 4-1. Table 4-1 shows examples of volatile DAC register values and the corresponding theoretical VOUT voltage for the MCP47X6 devices.

Note: When Gain = 2 (VRL = VREF), if VREF > V_DD/2, the VOUT voltage will be limited to V_DD. So if VREF = V_DD, then the VOUT voltage will not change for volatile DAC register values mid-scale and greater, since the op amp is at its full scale output.

EQUATION 4-1: CALCULATING OUTPUT VOLTAGE (VOUT)

VOUT = \frac{VRL \times DAC Register Value}{\# Resistors in Resistor Ladder} \times Gain

# Resistors in Resistor Ladder = 4096 (MCP4726)

1024 (MCP4716)

256 (MCP4706)

The DAC register value will be latched on the falling edge of the Acknowledge pulse of the Write command’s last byte. Then the VOUT voltage will start driving to the new value.

The following events update the analog voltage output (VOUT):

• Power-on Reset or General Call Reset command: Output is updated with EEPROM data.
• Falling edge of the Acknowledge pulse of the last Write command byte.

4.4.2.1 Resolution/Step Voltage

The Step voltage is dependent on the device resolution and the output voltage range. One LSB is defined as the ideal voltage difference between two successive codes. The step voltage can easily be calculated by using Equation 4-1 where the DAC register value is equal to 1.
4.4.3 OUTPUT SLEW RATE

Figure 4-5 shows an example of the slew rate of the \( V_{\text{OUT}} \) pin. The slew rate can be affected by the characteristics of the circuit connected to the \( V_{\text{OUT}} \) pin.

\[
\text{Slew Rate} = \frac{|V_{\text{OUT}(B)} - V_{\text{OUT}(A)}|}{\Delta T}
\]

**FIGURE 4-5:** \( V_{\text{OUT}} \) pin Slew Rate.

4.4.4 SMALL CAPACITIVE LOAD

With a small capacitive load, the output buffer’s current is not affected by the capacitive load \( (C_L) \). However, the \( V_{\text{OUT}} \) pin’s voltage is not a step transition from one output value (wiper code value) to the next output value. The change of the \( V_{\text{OUT}} \) voltage is limited by the output buffer’s characteristics, so the \( V_{\text{OUT}} \) pin voltage will have a slope from the old voltage to the new voltage. This slope is fixed for the output buffer, and is referred to as the buffer slew rate \( (S_{\text{BUF}}) \).

4.4.5 LARGE CAPACITIVE LOAD

With a larger capacitive load, the slew rate is determined by two factors:

- The output buffer’s short circuit current \( (I_{\text{SC}}) \)
- The \( V_{\text{OUT}} \) pin’s external load

\( I_{\text{OUT}} \) cannot exceed the output buffer’s short circuit current \( (I_{\text{SC}}) \) which fixes the output buffer slew rate (\( S_{\text{BUF}} \)). The voltage on the capacitive load \( (C_L) \), \( V_{\text{CL}} \), changes at a rate proportional to \( I_{\text{OUT}} \), which fixes a capacitive load slew rate \( (S_{\text{CL}}) \).

So the \( V_{\text{CL}} \) voltage slew rate is limited to the slower of the output buffer’s internally set slew rate \( (S_{\text{BUF}}) \) and the capacitive load slew rate \( (S_{\text{CL}}) \).

4.4.6 DRIVING RESISTIVE AND CAPACITIVE LOADS

The \( V_{\text{OUT}} \) pin can drive up to 100 pF of capacitive load in parallel with a 5 k\( \Omega \) resistive load (to meet electrical specifications). Figure 2-94 shows the \( V_{\text{OUT}} \) vs. Resistive Load.

\( V_{\text{OUT}} \) drops slowly as the load resistance decreases after about 3.5 k\( \Omega \). It is recommended to use a load with \( R_L \) greater than 5 k\( \Omega \).

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop’s phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response with overshoot and ringing in the step response. That is, since the \( V_{\text{OUT}} \) pin’s voltage does not quickly follow the buffer’s input voltage (due to the large capacitive load), the output buffer will overshoot the desired target voltage. Once the driver detects this overshoot, it compensates by forcing it to a voltage below the target. This causes voltage ringing on the \( V_{\text{OUT}} \) pin.

So, when driving large capacitive loads with the output buffer, a small series resistor \( (R_{\text{ISO}}) \) at the output (see Figure 4-6) improves the output buffer’s stability (feedback loop’s phase margin) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

\[
\text{FIGURE 4-6: Circuit to Stabilize Output Buffer for Large Capacitive Loads (C_L).}
\]

The \( R_{\text{ISO}} \) resistor value for your circuit needs to be selected. The resulting frequency response peaking and step response overshoot for this \( R_{\text{ISO}} \) resistor value should be verified on the bench. Modify the \( R_{\text{ISO}} \)’s resistance value until the output characteristics meet your requirements.

A method to evaluate the system’s performance is to inject a step voltage on the \( V_{\text{REF}} \) pin and observe the \( V_{\text{OUT}} \) pin’s characteristics.

**Note:** Additional insight into circuit design for driving capacitive loads can be found in AN884 “Driving Capacitive Loads With Op Amps” (DS00884).
TABLE 4-1: DAC INPUT CODE VS. ANALOG OUTPUT (V\text{OUT}) (V\text{DD} = 5.0V)

<table>
<thead>
<tr>
<th>Device</th>
<th>Volatile DAC Register Value</th>
<th>V\text{RL} (1)</th>
<th>LSb Gain Selection (2)</th>
<th>Gain Selection (2)</th>
<th>V\text{OUT} (4)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>5.0V/4096</td>
<td>1x</td>
<td>V\text{RL} * (4095/4096) * 1</td>
<td>4.998779</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.0V/4096</td>
<td>1x</td>
<td>V\text{RL} * (4095/4096) * 1</td>
<td>2.499390</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V/4096</td>
<td>2x (3)</td>
<td>V\text{RL} * (4095/4096) * 2</td>
<td>4.998779</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V/4096</td>
<td>1x</td>
<td>V\text{RL} * (2047/4096) * 1</td>
<td>2.498779</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V/4096</td>
<td>1x</td>
<td>V\text{RL} * (2047/4096) * 1</td>
<td>1.249390</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V/4096</td>
<td>2x (3)</td>
<td>V\text{RL} * (2047/4096) * 2</td>
<td>2.498779</td>
</tr>
<tr>
<td>MCP4726 (12-bit)</td>
<td></td>
<td>5.0V/2047</td>
<td>1x</td>
<td>V\text{RL} * (2047/2048) * 1</td>
<td>1.248779</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.0V/2047</td>
<td>1x</td>
<td>V\text{RL} * (1023/2048) * 1</td>
<td>0.624390</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.0V/2047</td>
<td>2x (3)</td>
<td>V\text{RL} * (1023/2048) * 2</td>
<td>1.248779</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V/1024</td>
<td>1x</td>
<td>V\text{RL} * (1023/1024) * 1</td>
<td>4.995117</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V/1024</td>
<td>1x</td>
<td>V\text{RL} * (1023/1024) * 1</td>
<td>2.497559</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V/1024</td>
<td>2x (3)</td>
<td>V\text{RL} * (1023/1024) * 2</td>
<td>4.995117</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.0V/511</td>
<td>1x</td>
<td>V\text{RL} * (511/1024) * 1</td>
<td>2.495117</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.0V/511</td>
<td>1x</td>
<td>V\text{RL} * (511/1024) * 1</td>
<td>1.247559</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.0V/511</td>
<td>2x (3)</td>
<td>V\text{RL} * (511/1024) * 2</td>
<td>2.495117</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V/255</td>
<td>1x</td>
<td>V\text{RL} * (255/1024) * 1</td>
<td>1.245117</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V/255</td>
<td>1x</td>
<td>V\text{RL} * (255/1024) * 1</td>
<td>0.622559</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V/255</td>
<td>2x (3)</td>
<td>V\text{RL} * (255/1024) * 2</td>
<td>1.245117</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.0V/127</td>
<td>1x</td>
<td>V\text{RL} * (127/256) * 1</td>
<td>1.240234</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.0V/127</td>
<td>1x</td>
<td>V\text{RL} * (127/256) * 1</td>
<td>0.615234</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.0V/127</td>
<td>2x (3)</td>
<td>V\text{RL} * (127/256) * 2</td>
<td>0.615234</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.0V/63</td>
<td>1x</td>
<td>V\text{RL} * (63/256) * 1</td>
<td>1.230469</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.0V/63</td>
<td>1x</td>
<td>V\text{RL} * (63/256) * 1</td>
<td>0.615234</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.0V/63</td>
<td>2x (3)</td>
<td>V\text{RL} * (63/256) * 2</td>
<td>1.230469</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.0V/0</td>
<td>1x</td>
<td>V\text{RL} * (0/256) * 1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.0V/0</td>
<td>1x</td>
<td>V\text{RL} * (0/256) * 1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.0V/0</td>
<td>2x (3)</td>
<td>V\text{RL} * (0/256) * 2</td>
<td>0</td>
</tr>
</tbody>
</table>

Note 1: V\text{RL} is the resistor ladder’s reference voltage. It is independent of V\text{REF}_1:V\text{REF}_0 selection.
2: Gain selection of 2x requires voltage reference source to come from V\text{REF} pin and requires V\text{REF} pin voltage ≤ V\text{DD} / 2.
3: Requires G = 1, V\text{REF}_1:V\text{REF}_0 = 10 or ‘11’, and V\text{RL} ≤ V\text{DD}/2.
4: These theoretical calculations do not take into account the Offset and Gain errors.
4.5 Power-Down Operation

To allow the application to conserve power when the DAC operation is not required, three Power-Down modes are available. The Power-Down Configuration bits (PD1:PD0) control the power-down operation (Figure 4-7). All Power-Down modes do the following:

- Turn off most of its internal circuits (op amp, resistor ladder, ...)
- Op amp output becomes high-impedance to the VOUT pin
- Disconnects resistor ladder from reference voltage (VRL)
- Retains the value of the volatile DAC register and Configuration bits, and the nonvolatile (EEPROM) DAC register and Configuration bits

Depending on the selected Power-Down mode, the following will occur:

- VOUT pin is switched to one of three resistive pull-downs (See Table 4-2)
  - 640kΩ (typical)
  - 125kΩ (typical)
  - 1kΩ (typical)

There is a delay (TPDE) between the PD1:PD0 bits changing from '00' to either '01', '10', or '11' and the op amp no longer driving the VOUT output and the pull-down resistors are sinking current.

In any of the Power-Down modes, where the VOUT pin is not externally connected (sinking or sourcing current), the power-down current will typically be 60 nA (see Section 1.0 “Electrical Characteristics”).

Section 6.0 “MCP47X6 I2C Commands” describes the I2C commands for writing the power-down bits. The commands that can update the volatile PD1:PD0 bits are:

- Write Volatile DAC Register
- Write Volatile Memory
- Write All Memory
- Write Volatile Configuration Bits
- General Call Reset
- General Call Wake-up

**Note:** The I2C serial interface circuit is not affected by the Power-Down mode. This circuit remains active in order to receive any command that might come from the I2C master device.

**TABLE 4-2: POWER-DOWN BITS AND OUTPUT RESISTIVE LOAD**

<table>
<thead>
<tr>
<th>PD1</th>
<th>PD0</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Normal operation</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1 kΩ resistor to ground</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>125 kΩ resistor to ground</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>640 kΩ resistor to ground</td>
</tr>
</tbody>
</table>

**FIGURE 4-7: Op Amp to VOUT Pin Block Diagram.**

4.5.1 EXITING POWER-DOWN

When the device exits the Power-Down mode, the following occurs:

- Disabled circuits (op amp, resistor ladder, ...) are turned on
- Resistor ladder is connected to selected reference voltage (VRL)
- Selected pull-down resistor is disconnected
- The VOUT output will be driven to the voltage represented by the volatile DAC register’s value and Configuration bits

The VOUT output signal will require time as these circuits are powered up and the output voltage is driven to the specified value as determined by the volatile DAC register and Configuration bits.

**Note:** Since the op amp and resistor ladder were powered off (0V), the op amp’s input voltage (VW) can be considered 0V. There is a delay (TPDD) between the PD1:PD0 bits updated to ‘00’ and the op amp driving the VOUT output. The op amp’s settling time (from 0V) needs to be taken into account to ensure the VOUT voltage reflects the selected value.

The following events will change the PD1:PD0 bits to ‘00’ and therefore exit the Power-Down mode. These are:

- Any I2C Write command for where the PD1:PD0 bits are ‘00’
- I2C General Call Wake-up Command
- I2C General Call Reset Command (if nonvolatile PD1:PD0 bits are ‘00’)
4.6 Device Resets

Device Resets can be grouped into two types: Resets due to change in voltage (POR/BOR Reset), and Resets caused by the system master (such as a microcontroller).

After a device Reset, and when $V_{DD} \geq V_{DD\text{(MIN)}}$, the device memory may be written or read.

4.6.1 POR/BOR RESET OPERATION

The POR and BOR trip points are at the same voltage, and are determined if the $V_{DD}$ voltage is rising or falling (see Figure 4-1). What occurs is different, depending if the Reset is a POR or BOR Reset.

**POR Reset (V_{DD} Rising)**

On a POR Reset, the nonvolatile memory values (DAC register and Configuration bits) are latched into the volatile memory. This configures the analog output ($V_{OUT}$) circuitry. A Reset delay timer also starts. During this delay time, the $\text{i}^2\text{C}$ interface will not accept commands.

**BOR Reset (V_{DD} Falling)**

On a BOR Reset, the device is forced into a power-down state. The volatile PD1:PD0 bits are forced to ‘11’ and all other volatile memory forced to ‘0’. The $\text{i}^2\text{C}$ interface will not accept commands.

4.6.2 RESET COMMANDS

When the MCP47X6 is in the valid operating voltage, the $\text{i}^2\text{C}$ General Call Reset command will force a Reset event. This is similar to the POR Reset, except that the Reset delay timer is not started.

In the case where the $\text{i}^2\text{C}$ interface bus does not seem to be responsive, the technique shown in Section 8.9 “Software I2C Interface Reset Sequence” can be used to force the $\text{i}^2\text{C}$ interface to be reset.

4.7 DAC Registers, Configuration Bits, and Status Bits

The MCP47X6 devices have both volatile and nonvolatile (EEPROM) memory. Figure 4-8 shows the volatile and nonvolatile memory and their interaction due to a POR event.

There are five Configuration bits in both the volatile and nonvolatile memory, the DAC registers in both the volatile and nonvolatile memory, and two volatile Status bits. The DAC registers (volatile and nonvolatile) will be either 12-bits (MCP4726), 10-bits (MCP4716), or 8-bits (MCP4706) wide.

When the device is first powered up, it automatically uploads the EEPROM memory values to the volatile memory. The volatile memory determines the analog output ($V_{OUT}$) pin voltage. After the device is powered up, the user can update the device memory.

The $\text{i}^2\text{C}$ interface is how this memory is read and written. Refer to Section 5.0 “$\text{i}^2\text{C} \text{ Serial Interface}” and Section 6.0 “MCP47X6 $\text{i}^2\text{C} \text{ Commands}” for more details on the reading and writing the device’s memory.

When the nonvolatile memory is written (using the $\text{i}^2\text{C}$ Write All Memory command), the volatile memory is written with the same values. The device starts writing the EEPROM cell at the Acknowledge pulse of the EEPROM Write command.

Table 4-3 shows the operation of the device Status bits, Table 4-4 shows the operation of the device Configuration bits, and Table 4-5 shows the factory default value of a POR/BOR event for the device Configuration bits.

There are two Status bits. These are only in volatile memory and give indication on the status of the device. The POR bit indicates if the device $V_{DD}$ is above or below the POR trip point. During normal operation, this bit should be ‘1’. The RDY/BSY bit indicates if an EEPROM write cycle is in progress. While the RDY/BSY bit is low (during the EEPROM writing), all commands are ignored, except for the Read command.

---

**FIGURE 4-8:** DAC Memory and POR Interaction.
### TABLE 4-3: STATUS BITS OPERATION

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RDY/BSY</td>
<td>This bit indicates the state of the EEPROM program memory&lt;br&gt; 1 = EEPROM is not in a programming cycle&lt;br&gt; 0 = EEPROM is in a programming cycle</td>
</tr>
<tr>
<td>POR</td>
<td>Power-on Reset Status Indicator (flag)&lt;br&gt; 1 = Device is powered on with VDD &gt; VPOR.&lt;br&gt; Ensure that VDD is above VDD(MIN) to ensure proper operation.&lt;br&gt; 0 = Device is in powered off state. If this value is read, VDD &lt; VDD(MIN) &lt; VPOR. Unreliable device operation should be expected.</td>
</tr>
</tbody>
</table>

### TABLE 4-4: CONFIGURATION BITS

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>VREF1:VREF0</td>
<td>Resistor Ladder Voltage Reference (VRL) Selection bits&lt;br&gt; 0x = VDD (Unbuffered)&lt;br&gt; 10 = VREF pin (Unbuffered)&lt;br&gt; 11 = VREF pin (Buffered)</td>
</tr>
<tr>
<td>PD1:PD0</td>
<td>Power-Down Selection bits&lt;br&gt; When the DAC is powered down, most of the internal circuits are powered off and the op amp is disconnected from the VOUT pin.&lt;br&gt; 00 = Not Powered Down (Normal operation)&lt;br&gt; 01 = Powered Down – VOUT is loaded with 1 kΩ resistor to ground.&lt;br&gt; 10 = Powered Down – VOUT is loaded with 100 kΩ resistor to ground.&lt;br&gt; 11 = Powered Down – VOUT is loaded with 500 kΩ resistor to ground.</td>
</tr>
<tr>
<td>G</td>
<td>Gain Selection bit&lt;br&gt; 0 = 1x (gain of 1)&lt;br&gt; 1 = 2x (gain of 2). Not applicable when VDD is used as VRL</td>
</tr>
</tbody>
</table>

**Note:** See Table 4-2 and Figure 4-7 for more details.

### TABLE 4-5: CONFIGURATION BIT VALUES AFTER POR/BOR EVENT

<table>
<thead>
<tr>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VREF1</td>
<td>VREF0</td>
<td>PD1</td>
<td>PD0</td>
<td>G</td>
<td></td>
</tr>
<tr>
<td>POR Event</td>
<td>0 (1)</td>
<td>0 (1)</td>
<td>0 (1)</td>
<td>0 (1)</td>
<td>0 (1)</td>
<td>When VDD transitions from VDD &lt; VPOR to VDD &gt; VPOR</td>
</tr>
<tr>
<td>BOR Event</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>When VDD transitions from VDD &gt; VBOR to VDD &lt; VBOR</td>
</tr>
</tbody>
</table>

**Note 1:** Default configuration when the device is shipped to customer. The POR/BOR value may be modified by writing the corresponding nonvolatile Configuration bit.

### REGISTER 4-1: DAC REGISTER BITS

<table>
<thead>
<tr>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td></td>
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<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>D9</td>
<td>D8</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>D11</td>
<td>D10</td>
<td>D9</td>
<td>D8</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>POR/BOR Event</td>
<td>0 (1)</td>
<td>0 (1)</td>
<td>0 (1)</td>
<td>0 (1)</td>
<td>0 (1)</td>
<td>0 (1)</td>
<td>0 (1)</td>
<td>0 (1)</td>
<td>0 (1)</td>
<td>0 (1)</td>
<td>0 (1)</td>
<td>0 (1)</td>
</tr>
</tbody>
</table>

**Note 1:** Default configuration when the device is shipped to customer. The POR/BOR value may be modified by writing the corresponding nonvolatile Configuration bit.

**Note 2:** This device does not implement this bit, so there is no corresponding POR/BOR value.
5.0 I²C SERIAL INTERFACE

The MCP47X6 devices support the I²C serial protocol. The MCP47X6 I²C’s module operates in Slave mode (does not generate the serial clock).

5.1 Overview

This I²C interface is a two-wire interface. Figure 5-1 shows a typical I²C interface connection.

The I²C interface specifies different communication bit rates. These are referred to as Standard, Fast or High-Speed modes. The MCP47X6 supports these three modes. The bit rates of these modes are:
• Standard mode: bit rates up to 100 kbit/s
• Fast mode: bit rates up to 400 kbit/s
• High-Speed mode (HS mode): bit rates up to 3.4 Mbit/s

A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the Start and Stop conditions. The MCP47X6 device works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. Communication is initiated by the master (microcontroller) which sends the Start bit, followed by the slave address byte. The first byte transmitted is always the slave address byte, which contains the device code, the address bits, and the R/W bit.

5.2 Signal Descriptions

The I²C interface uses up to two pins (signals). These are:
• SDA (Serial Data)
• SCL (Serial Clock)

5.2.1 SERIAL DATA (SDA)

The Serial Data (SDA) signal is the data signal of the device. The value on this pin is latched on the rising edge of the SCL signal when the signal is an input.

With the exception of the Start and Stop conditions, the high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. During the high period of the clock, the SDA pin’s value (high or low) must be stable. Changes in the SDA pin’s value while the SCL pin is High will be interpreted as a Start or a Stop condition.

5.2.2 SERIAL CLOCK (SCL)

The Serial Clock (SCL) signal is the clock signal of the device. The rising edge of the SCL signal latches the value on the SDA pin.

The MCP47X6 will not stretch the clock signal (SCL) since memory read access occurs fast enough.

Depending on the clock rate mode, the interface will display different characteristics.

![Typical I²C Interface Connections](image)

The I²C serial protocol only defines the field types, field lengths, timings, etc. of a frame. The frame content defines the behavior of the device. For details on the frame content (commands/data) refer to Section 6.0 “MCP47X6 I²C Commands”.

Refer to the NXP I²C document for more details on the I²C specifications.
5.3 I\(^2\)C Operation

The MCP47X6's I\(^2\)C module is compatible with the NXP I\(^2\)C specification. The following lists some of the module's features:

- 7-bit slave addressing
- Supports three clock rate modes:
  - Standard mode, clock rates up to 100 kHz
  - Fast mode, clock rates up to 400 kHz
  - High-speed mode (HS mode), clock rates up to 3.4 MHz
- Support multi-master applications
- General call addressing (Reset and Wake-Up commands)

The I\(^2\)C 10-bit Addressing mode is not supported.

The NXP I\(^2\)C specification only defines the field types, field lengths, timings, etc. of a frame. The frame content defines the behavior of the device. The frame content for the MCP47X6 is defined in Section 6.0 “MCP47X6 I\(^2\)C Commands”.

5.3.1 I\(^2\)C BIT STATES AND SEQUENCE

Figure 5-8 shows the I\(^2\)C transfer sequence. The serial clock is generated by the master. The following definitions are used for the bit states:

- Start bit (S)
- Data bit
- Acknowledge (A) bit (driven low) / No Acknowledge (A) bit (not driven low)
- Repeated Start bit (Sr)
- Stop bit (P)

5.3.1.1 Start Bit

The Start bit (see Figure 5-2) indicates the beginning of a data transfer sequence. The Start bit is defined as the SDA signal falling when the SCL signal is “High”.

5.3.1.2 Data Bit

The SDA signal may change state while the SCL signal is Low. While the SCL signal is High, the SDA signal MUST be stable (see Figure 5-3).

5.3.1.3 Acknowledge (A) Bit

The A bit (see Figure 5-4) is typically a response from the receiving device to the transmitting device. Depending on the context of the transfer sequence, the A bit may indicate different things. Typically, the slave device will supply an A response after the Start bit and 8 "data" bits have been received. An A bit has the SDA signal low.

![](SDA.png) ![](D0.png) ![](A.png) ![](SCL.png)

**FIGURE 5-4: Acknowledge Waveform.**

Not A (A\(~\)) Response

The A\(~\) bit has the SDA signal high. Table 5-1 shows some of the conditions where the slave device will issue a Not A (A\(~\)).

If an error condition occurs (such as an A\(~\) instead of A), then a Start bit must be issued to reset the command state machine.

<table>
<thead>
<tr>
<th>Event</th>
<th>Acknowledge Bit Response</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>General Call</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Slave Address valid</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Slave Address not valid</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Communication during EEPROM write cycle</td>
<td>A</td>
<td>After device has received address and command, and valid conditions for EEPROM write</td>
</tr>
<tr>
<td>Bus Collision</td>
<td>N/A</td>
<td>(I^2C) module Resets, or a “Don't Care” if the collision occurs on the Master’s “Start bit”</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Event</th>
<th>Acknowledge Bit Response</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>General Call</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Slave Address valid</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Slave Address not valid</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Communication during EEPROM write cycle</td>
<td>A</td>
<td>After device has received address and command, and valid conditions for EEPROM write</td>
</tr>
<tr>
<td>Bus Collision</td>
<td>N/A</td>
<td>(I^2C) module Resets, or a “Don't Care” if the collision occurs on the Master’s “Start bit”</td>
</tr>
</tbody>
</table>
5.3.1.4 Repeated Start Bit

The Repeated Start bit (see Figure 5-5) indicates the current master device wishes to continue communicating with the current slave device without releasing the I²C bus. The Repeated Start condition is the same as the Start condition, except that the Repeated Start bit follows a Start bit (with the Data bits + A bit) and not a Stop bit.

The Start bit is the beginning of a data transfer sequence and is defined as the SDA signal falling when the SCL signal is “High”.

Note 1: A bus collision during the Repeated Start condition occurs if:
- SDA is sampled low when SCL goes from low to high.
- SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data "1".

5.3.1.5 Stop Bit

The Stop bit (see Figure 5-6) indicates the end of the I²C Data Transfer Sequence. The Stop bit is defined as the SDA signal rising when the SCL signal is “High”.

A Stop bit resets the I²C interface of all MCP47X6 devices.

5.3.2 CLOCK STRETCHING

“Clock Stretching” is something that the receiving Device can do, to allow additional time to “respond” to the “data” that has been received.

The MCP47X6 will not stretch the clock signal (SCL) since memory read access occurs fast enough.

5.3.3 ABORTING A TRANSMISSION

If any part of the I²C transmission does not meet the command format, it is aborted. This can be intentionally accomplished with a Start or Stop condition. This is done so that noisy transmissions (usually an extra Start or Stop condition) are aborted before they corrupt the device.
5.3.4 SLOPE CONTROL

The MCP47X6 implements slope control on the SDA output.

As the device transitions from HS mode to FS mode, the slope control parameter will change from the HS specification to the FS specification.

For Fast (FS) and High-Speed (HS) modes, the device has a spike suppression and a Schmidt Trigger at SDA and SCL inputs.

5.3.5 DEVICE ADDRESSING

The address byte is the first byte received following the Start condition from the master device. The MCP47X6's slave address consists of a 4-bit fixed code ('1100') and a 3-bit code that is user specified when the device is ordered. This allows up to eight MCP47X6 devices on a single I²C bus.

Figure 5-9 shows the I²C slave address byte format, which contains the seven address bits and a read/write (R/W) bit. Table 5-2 shows the eight I²C slave address options and their respective device order code.

<table>
<thead>
<tr>
<th>7-bit I²C Address</th>
<th>Device Order Code</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>'1100000'</td>
<td>MCP47x6A0-E/xx</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MCP47x6A0T-E/xx</td>
<td>Tape and Reel</td>
</tr>
<tr>
<td>'1100001'</td>
<td>MCP47x6A1-E/xx</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MCP47x6A1T-E/xx</td>
<td>Tape and Reel</td>
</tr>
<tr>
<td>'1100010'</td>
<td>MCP47x6A2-E/xx</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MCP47x6A2T-E/xx</td>
<td>Tape and Reel</td>
</tr>
<tr>
<td>'1100011'</td>
<td>MCP47x6A3-E/xx</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MCP47x6A3T-E/xx</td>
<td>Tape and Reel</td>
</tr>
<tr>
<td>'1100100'</td>
<td>MCP47x6A4-E/xx</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MCP47x6A4T-E/xx</td>
<td>Tape and Reel</td>
</tr>
<tr>
<td>'1100101'</td>
<td>MCP47x6A5-E/xx</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MCP47x6A5T-E/xx</td>
<td>Tape and Reel</td>
</tr>
<tr>
<td>'1100110'</td>
<td>MCP47x6A6-E/xx</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MCP47x6A6T-E/xx</td>
<td>Tape and Reel</td>
</tr>
<tr>
<td>'1100111'</td>
<td>MCP47x6A7-E/xx</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MCP47x6A7T-E/xx</td>
<td>Tape and Reel</td>
</tr>
</tbody>
</table>

Note 1: The sample center will generally stock I²C address '1100000', other addresses may be available.

Note 2: 'xx' in the order code is the device package code (CH for SOT-23 and MAY for DFN)
5.3.6 HS MODE

The I2C specification requires that a High-Speed mode device must be ‘activated’ to operate in High-Speed (3.4 Mbit/s) mode. This is done by the master sending a special address byte following the Start bit. This byte is referred to as the High-Speed Master Mode Code (HSMMC).

The MCP47X6 device does not acknowledge this byte. However, upon receiving this command, the device switches to HS mode. The device can now communicate at up to 3.4 Mbit/s on SDA and SCL lines. The device will switch out of the HS mode on the next Stop condition.

The master code is sent as follows:
1. Start condition (S)
2. High-Speed Master Mode Code (0000 1XXX), The XXX bits are unique to the High-Speed (HS) mode master.
3. No Acknowledge (Ā)

After switching to the High-Speed mode, the next transferred byte is the I2C control byte, which specifies the device to communicate with, and any number of data bytes plus acknowledgements. The master device can then either issue a Repeated Start bit to address a different device (at High-Speed) or a Stop bit to return to Fast/Standard bus speed. After the Stop bit, any other master device (in a multi-master system) can arbitrate for the I2C bus.

See Figure 5-10 for illustration of HS mode command sequence.

For more information on the HS mode, or other I2C modes, please refer to the NXP I2C specification.

5.3.6.1 Slope Control

The slope control on the SDA output is different between the Fast/Standard Speed and the High-Speed clock modes of the interface.

5.3.6.2 Pulse Gobbler

The pulse gobbler on the SCL pin is automatically adjusted to suppress spikes < 10 ns during HS mode.

---

**FIGURE 5-10:** HS Mode Sequence.

- S = Start bit
- Sr = Repeated Start bit
- Ā = Acknowledge bit
- Ā = Not Acknowledge bit
- R/W = Read/Write bit
- P = Stop bit (Stop condition terminates HS mode)
5.3.7 GENERAL CALL

The General Call is a method that the “master” device can communicate with all other “slave” devices. In a multi-master application, the other master devices are operating in Slave mode. The General Call address has two documented formats. These are shown in Figure 5-11.

The MCP47X6 has two General Call commands. The function of these commands are:

- Reset the device(s) (Software Reset)
- Wake-Up the device(s)

For details on the operation of the MCP47X6’s General Call commands, see Section 6.6 “I2C General Call Commands”.

**Note:** Only one General Call command per issue of the General Call control byte. Any additional General Call commands are ignored and Not Acknowledged.

**FIGURE 5-11:** General Call Formats.
6.0 MCP47X6 I\(^2\)C COMMANDS

The I\(^2\)C protocol does not specify how commands are formatted, so this section specifies the MCP47X6’s I\(^2\)C command formats and operation.

The commands can be grouped into the following categories:

- Write memory
- Read memory
- General Call commands

The supported commands are shown in Table 6-2. Many of these commands allow for continuous operation. This means that the I\(^2\)C master does not generate a Stop bit but repeats the required data/clocks. This allows faster updates since the overhead of the I\(^2\)C control byte is removed. Table 6-1 shows the supported commands and the required number of bit clocks for both single and continuous commands.

Write commands, determined by the R/W bit = 0, use up to three command codes bits (C2:C0) to determine the write’s operation.

The Read command is strictly determined by the R/W bit = 1. There are two formats of the command, one for 12-bit and 10-bit devices and a second for 8-bit devices.

The General Call commands utilize the I\(^2\)C specification reserved General Call command address and command codes.

### Table 6-1: I\(^2\)C COMMANDS - NUMBER OF CLOCKS

<table>
<thead>
<tr>
<th>Command Name</th>
<th>Operation</th>
<th>Mode</th>
<th>Clocks ((n))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write Volatile DAC Register Command ((\text{Note 2}))</td>
<td>Single</td>
<td></td>
<td>29</td>
</tr>
<tr>
<td>Write Volatile Memory Command</td>
<td>Single</td>
<td></td>
<td>38</td>
</tr>
<tr>
<td>Write All Memory Command</td>
<td>Single</td>
<td></td>
<td>38</td>
</tr>
<tr>
<td>Write Volatile Configuration Bits Command</td>
<td>Single</td>
<td></td>
<td>20</td>
</tr>
<tr>
<td>Read Command (12 and 10-bit DAC Register) ((\text{Note 2}))</td>
<td>Single</td>
<td></td>
<td>65</td>
</tr>
<tr>
<td>Read Command (8-bit DAC Register) ((\text{Note 2}))</td>
<td>Single</td>
<td></td>
<td>47</td>
</tr>
<tr>
<td>Write Volatile DAC Register Command</td>
<td>Continuous</td>
<td>(18n + 11)</td>
<td></td>
</tr>
<tr>
<td>Write Volatile Memory Command</td>
<td>Continuous</td>
<td>(27n + 11)</td>
<td></td>
</tr>
<tr>
<td>Write All Memory Command</td>
<td>Continuous</td>
<td>(27n + 11)</td>
<td></td>
</tr>
<tr>
<td>Write Volatile Configuration Bits Command</td>
<td>Continuous</td>
<td>(9n + 11)</td>
<td></td>
</tr>
<tr>
<td>Read Command (12 and 10-bit DAC Register) ((\text{Note 2}))</td>
<td>Continuous</td>
<td>(54n + 11)</td>
<td></td>
</tr>
<tr>
<td>Read Command (8-bit DAC Register) ((\text{Note 2}))</td>
<td>Continuous</td>
<td>(36n + 11)</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: "\(n\)" indicates the number of times the command operation is to be repeated.

Note 2: This command is useful to determine when an EEPROM programming cycle has completed (RDY/BSY Status bit)

### Table 6-2: MCP47X6 SUPPORTED COMMANDS

<table>
<thead>
<tr>
<th>Command Code ((\text{Note 1}))</th>
<th>Command Name</th>
<th>Writes Volatile Memory?</th>
<th>Writes EEPROM Memory?</th>
<th>Command during EEPROM Write Cycle?</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2 C1 C0</td>
<td>PD1:PD0 only</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Writes volatile power-down bits so can also be used to exit a power-down state.</td>
</tr>
<tr>
<td>0 0 X</td>
<td>Write Volatile DAC Register Command ((\text{Note 2}))</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>0 1 0</td>
<td>Write Volatile Memory Command</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>0 1 1</td>
<td>Write All Memory Command</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>1 0 0</td>
<td>Write Volatile Configuration Bits Command</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>1 0 1</td>
<td>Reserved</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>Reserved ((\text{Note 3}))</td>
</tr>
<tr>
<td>1 1 0</td>
<td>Read Command</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>Determined by R/W bit in I(^2)C™ Control byte</td>
</tr>
<tr>
<td>1 1 1</td>
<td>General Call Reset</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>Determined by General Call command byte after the I(^2)C General Call address.</td>
</tr>
<tr>
<td></td>
<td>General Call Wake-up</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: These bits are the MSb of the 2nd byte in the I\(^2\)C Write command. See Figure 6-1 to Figure 6-4.

Note 2: X = Don’t Care bit. This command format does not use C0 bit.

Note 3: Device operation is not specified.
6.1 Write Volatile DAC Register  
(C2:C0 = 00x)

This command is used to update the volatile DAC register value and the two Power-down Configuration bits (PD1:PD0). This command is typically used for a quick update of the analog output by modifying the minimum parameters. The EEPROM values are not affected by this command.

Figure 6-1 shows an example of the command format, where a Stop bit completes the command.

The volatile DAC register and Power-down Configuration bits are updated with the written data at the completion of the ACK bit (falling edge of SCL).

After this ACK bit, the \(^{2}\)C master should generate a Stop bit or the \(^{2}\)C master can repeat the 2nd (2 command bits + 2 power-down bits + 4 data bits (b11:b08)) and the 3rd byte (8 data bits (b07:b00)). Repeating the 2nd and 3rd bytes allows a continuous command where the volatile DAC register can be updated without the communication overhead of the device addressing byte (1st byte).

The device updates the \(V_{OUT}\) at the falling edge of the Acknowledge pulse of the 3rd byte.

Note 1: The device updates \(V_{OUT}\) at the falling edge of the SCL at the end of this ACK pulse.

2: The 2nd-3rd bytes can be repeated after the 3rd byte by continued clocking before issuing Stop bit.

3: ACK bit generated by MCP47X6.

Legend:
- \(x\) = don’t care
- D11:D00 = 12-bit data for MCP4726 device
- D09:D00 = 10-bit data for MCP4716 device
- D07:D00 = 8-bit data for MCP4706 device

FIGURE 6-1: Write Volatile DAC Register Command.
6.2 Write Volatile Memory
(C2:C0 = 010)

This Write command is used to update the volatile DAC register value and Configuration bits. The EEPROM is not affected by this command. Figure 6-2 shows an example of this Write command.

The volatile DAC register and Configuration bits are updated with the written date at the completion of the ACK bit (falling edge of SCL).

After this ACK bit, the I^2C master should generate a Stop bit or the I^2C master can repeat the 2nd (3 command bits + 5 Configuration bits), and the 3rd byte (8 data bits (b15:b08)), and the 4th byte (8 data bits (b07:b00)). Repeating the 2nd through 4th bytes allows a continuous command where the volatile DAC register and Configuration bits can be updated without the communication overhead of the device addressing byte (1st byte).

Note 1: The device updates VOUT at the falling edge of the SCL at the end of this ACK pulse.

2: The 2nd-4th bytes can be repeated after the 4th byte by continued clocking before issuing Stop bit.

3: ACK bit generated by MCP47X6.

Legend:
- X = don’t care
- D11:D00 = 12-bit data for MCP4726 device
- D09:D00 = 10-bit data for MCP4716 device
- D07:D00 = 8-bit data for MCP4706 device

FIGURE 6-2: Write Volatile Memory Command.
6.3 Write All Memory
(C2:C0 = 011)

This Write command is used to update the volatile and nonvolatile (EEPROM) DAC register value and Configuration bits. Figure 6-3 shows an example of this Write command.

- **V\text{OUT}** update: At the falling edge of the Acknowledge pulse of the 4th byte.
- **EEPROM update**: At the falling edge of the Acknowledge pulse of the 4th byte.

The DAC register and Power-down Configuration bits (volatile and EEPROM) are updated with the written date at the completion of the ACK bit (falling edge of SCL). The EEPROM memory requires time ($T_{WC}$) for the values to be written. Another Write All Memory command should not be issued until the EEPROM write is complete.

**Note:** RDY/BSY bit toggles to "low" and back to "high" after the EEPROM write is completed. The state of the RDY/BSY bit can be monitored by a Read command.

Write commands which only update volatile memory (C2:C0 = 00x or '010') can be issued. Read commands and the General Call commands may not be issued.

---

**FIGURE 6-3:** Write All Memory Command.

---

**Note 1:** The device updates $V\text{OUT}$ at the falling edge of the SCL at the end of this ACK pulse.

2: The 2nd-4th bytes can be repeated after the 4th byte by continued clocking before issuing Stop bit.

3: ACK bit generated by MCP47X6.

**Legend:**

- $x$ = don't care
- D11:D00 = 12-bit data for MCP4726 device
- D09:D00 = 10-bit data for MCP4716 device
- D07:D00 = 8-bit data for MCP4706 device

---

**Legend:**

- A = ACK
- V = Voltage
- G = Gain
6.4 Write Volatile Configuration Bits
(C2:C0 = 100)

This Write command is used to update the volatile Configuration register bits only. This command is a quick method to modify the configuration of the DAC, such as the selection of the resistor ladder reference voltage, the op amp gain, and the power-down state. Figure 6-4 shows an example of this Write command.

Note 1: The device updates VOUT at the falling edge of the SCL at the end of this ACK pulse.
2: The 2nd byte can be repeated after the 2nd by continued clocking before issuing Stop bit.
3: ACK bit generated by MCP47X6.

FIGURE 6-4: Write Volatile Configuration Bits Command.
6.5 READ COMMAND

This command reads all the device memory. This includes the volatile and nonvolatile (EEPROM) DAC register values and Configuration bits, and the volatile status bits.

This command is executed when the I²C control byte’s Read/Write bit is a ‘1’ (read).

This command has two different formats based on the resolution of the device. The 12-bit and 10-bit devices use the format in Figure 6-5, while the 8-bit device uses the format in Figure 6-6.

The 2nd byte (Configuration bits) indicates the current condition of the device operation. The RDY/BSY bit indicates EEPROM writing status.

FIGURE 6-5: Read Command Format for 12-bit DAC (MCP4726) and 10-bit DAC (MCP4716).
FIGURE 6-6: Read Command Format for 8-bit DAC (MCP4706).

Note 1: The 2nd-5th bytes can be repeated after the 5th byte by continued clocking before issuing Stop bit.

- 3: ACK bit generated by I²C™ master.
- 4: ACK/NACK bit generated by I²C™ master.

Legend: D07:D00 = 8-bit data for MCP4706 device
6.6 I²C General Call Commands

The device acknowledges the General Call Address command (0x00 in the first byte). The meaning of the general call address is always specified in the second byte. The I²C specification does not allow "00000000" (00h) in the second byte. Please refer to the Phillips I²C document for more details on the General Call specifications.

The MCP47X6 devices support the following I²C general calls:
- General Call Reset
- General Call Wake-Up

6.6.1 GENERAL CALL RESET

The device performs General Call Reset if the second byte is "00000110" (06h). At the acknowledgement of this byte, the device will abort the current conversion and perform the following tasks:

- Internal Reset similar to a Power-on Reset (POR).
  The contents of the EEPROM are loaded into the DAC registers and analog output is available immediately.
- This is a similar event to the POR. The VOUT will be available immediately, but after a short time delay following the Acknowledgement pulse. The VOUT value is determined by the EEPROM contents.

This command allows multiple MCP47X6 devices to be reset synchronously.

**FIGURE 6-7:** General Call Reset Command.

**Note 1:** At the falling edge of the SCL at the end of this ACK pulse a Reset occurs (start-up timer starts and DAC register latched).

**Note 2:** The 2nd byte can be repeated after the 2nd byte continued clocking before issuing Stop bit.

**Note 3:** ACK bit generated by MCP47X6.
6.6.2 GENERAL CALL WAKE-UP

If the second byte is "00001001" (09h), the device forces the volatile power-down bits to '00'. The nonvolatile (EEPROM) power-down bit values are not affected by this command.

This command allows multiple MCP47X6 devices to wake-up synchronously.

**FIGURE 6-8:** General Call Wake-Up Command.

![Diagram of General Call Wake-Up Command]

**Note:** This command does not adhere to the I2C specification where if the LSb of the 2nd byte is a '1', it is a 'Hardware General Call' (see the NXP I2C Specification).

**Note 1:** At the falling edge of the SCL, at the end of this ACK pulse, the volatile PD1:PD0 bits are forced to '00'.

1: The 2nd byte can be repeated after the 2nd by continued clocking before issuing Stop bit.
2: ACK bit generated by MCP47X6.
7.0 TERMINOLOGY

7.1 Resolution

The resolution is the number of DAC output states that divide the full-scale range. For the 12-bit DAC, the resolution is $2^{12}$, meaning the DAC code ranges from 0 to 4095.

7.2 Least Significant bit (LSb)

Normally this is thought of as the ideal voltage difference between two successive codes. This bit has the smallest value or weight of all bits in the register. For a given output voltage range, which is typically the voltage between the Full-Scale voltage and the Zero-Scale voltage ($V_{OUT(FS)} - V_{OUT(ZS)}$), it is divided by the resolution of the device (Equation 7-1).

**EQUATION 7-1: LSb VOLTAGE CALCULATION**

$$V_{LSb} = \frac{V_{OUT(FS)} - V_{OUT(ZS)}}{2^N - 1}$$

$2^N = 4096$ (MCP4726)

$1024$ (MCP4716)

$256$ (MCP4706)

7.3 Monotonicity

Normally this is thought of as the $V_{OUT}$ voltage never decreasing, as the DAC register code is continuously incremented by 1 code step (LSb).

7.4 Full-Scale Error (FSE)

The Full-Scale error (see Figure 7-4) is the sum of Offset error plus Gain error. It is the difference between the ideal and measured DAC output voltage with all bits set to one (DAC input code = FFFh for 12-bit DAC).

**EQUATION 7-2: FULL-SCALE ERROR**

$$FSE = \frac{V_{OUT(@FS)} - V_{IDEAL(@FS)}}{V_{LSb}}$$

Where:

- FSE is expressed in LSb
- $V_{OUT(@FS)}$ is the $V_{OUT}$ voltage when the DAC register code is at Full-scale.
- $V_{IDEAL(@FS)}$ is the ideal output voltage when the DAC register code is at Full-scale.
- $V_{LSb}$ is the delta voltage of one DAC register code step (such as code 000h to code 001h).

7.5 Zero-Scale Error (ZSE)

The Zero-Scale error (see Figure 7-4) is the difference between the ideal and measured $V_{OUT}$ voltage with the volatile DAC register equal to 000h. The Zero-Scale error is the same as the Offset error for this case (volatile DAC register = 000h).

**EQUATION 7-3: ZERO-SCALE ERROR**

$$ZSE = \frac{V_{OUT(@ZS)}}{V_{LSb}}$$

Where:

- FSE is expressed in LSb
- $V_{OUT(@ZS)}$ is the $V_{OUT}$ voltage when the DAC register code is at Zero-scale.
- $V_{LSb}$ is the delta voltage of one DAC register code step (such as code 000h to code 001h).

7.6 Offset Error

The Offset error (see Figure 7-1) is the deviation from zero voltage output when the volatile DAC register value = 000h (zero scale voltage). This error affects all codes by the same amount. The Offset error can be calibrated by software in application circuits.
7.7 Integral Nonlinearity (INL)

The Integral Nonlinearity (INL) error is the maximum deviation of an actual transfer function from an ideal transfer function (straight line).

In the MCP47X6, INL is calculated using two end points (zero and full scale). INL can be expressed as a percentage of full scale range (FSR) or in a fraction of an LSb. INL is also called relative accuracy. Equation 7-4 shows how to calculate the INL error in LSb and Figure 7-2 shows an example of INL accuracy.

**EQUATION 7-4: INL ERROR**

\[
INL = \frac{(V_{OUT} - V_{ideal})}{\text{LSb}}
\]

Where:
- INL is expressed in LSb.
- \(V_{ideal} = \text{Code} \times \text{LSb}\)
- \(V_{OUT} = \) The output voltage measured with a given DAC input code

**FIGURE 7-2: INL Accuracy Example.**

7.8 Differential Nonlinearity (DNL)

The Differential Nonlinearity (DNL) error (see Figure 7-3) is the measure of step size between codes in actual transfer function. The ideal step size between codes is 1 LSb. A DNL error of zero would imply that every code is exactly 1 LSb wide. If the DNL error is less than 1 LSb, the DAC ensures monotonic output and no missing codes. The DNL error between any two adjacent codes is calculated as follows:

**EQUATION 7-5: DNL ERROR**

\[
DNL = \frac{\Delta V_{OUT}}{\text{LSb}}
\]

Where:
- DNL is expressed in LSb.
- \(\Delta V_{OUT} = \) The measured DAC output voltage difference between two adjacent input codes

**FIGURE 7-3: DNL Accuracy Example.**
7.9 Gain Error

The Gain error (see Figure 7-4) is the difference between the actual full-scale output voltage from the ideal output voltage of the DAC transfer curve. The Gain error is calculated after nullifying the Offset error, or Full-Scale error minus the Offset error.

The Gain error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The Gain error is usually expressed as percent of full-scale range (% of FSR) or in LSb.

In the MCP4706/4716/4726, the Gain error is not calibrated at the factory and most of the Gain error is contributed by the output buffer (op amp) saturation near the code range beyond 4000d. For the applications that need the Gain error specification less than 1% maximum, the user may consider using the DAC code range between 100d and 4000d instead of using full code range (code 0 to 4095d). The DAC output of the code range between 100d and 4000d is much more linear than full-scale range (0 to 4095d). The Gain error can be calibrated out by software in the application.

7.10 Gain Error Drift

The Gain error drift is the variation in Gain error due to a change in ambient temperature. The Gain error drift is typically expressed in ppm/oC.

7.11 Offset Error Drift

The Offset error drift is the variation in Offset error due to a change in ambient temperature. The Offset error drift is typically expressed in ppm/oC.

7.12 Settling Time

The Settling time is the time delay required for the $V_{OUT}$ voltage to settle into its new output value. This time is measured from the start of code transition, to when the $V_{OUT}$ voltage is within the specified accuracy.

In the MCP47X6, the settling time is a measure of the time delay until the $V_{OUT}$ voltage reaches within 0.5 LSb of its final value, when the volatile DAC register changes from 400h to C00h.

7.13 Major-Code Transition Glitch

Major-code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-Sec, and is measured when the digital code is changed by 1 LSb at the major carry transition (Example: 011...111 to 100...000, or 100...000 to 011...111).

7.14 Digital Feedthrough

The digital feedthrough is the glitch that appears at the analog output caused by coupling from the digital input pins of the device. The area of the glitch is expressed in nV-Sec, and is measured with a full scale change (Example: all 0s to all 1s and vice versa) on the digital input pins. The digital feedthrough is measured when the DAC is not being written to the output register.

7.15 Power-Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in $V_{OUT}$ to a change in $V_{DD}$ for full-scale output of the DAC. The $V_{OUT}$ is measured while the $V_{DD}$ is varied +/- 10%, and expressed in dB or µV/V.
8.0 TYPICAL APPLICATIONS

The MCP47X6 family of devices are general purpose, single channel voltage output DACs for various applications where a precision operation with low-power and nonvolatile EEPROM memory is needed.

Since the devices include a nonvolatile EEPROM memory, the user can utilize these devices for applications that require the output to return to the previous set-up value on subsequent power-ups.

Applications generally suited for the devices are:
- Set Point or Offset Trimming
- Sensor Calibration
- Portable Instrumentation (Battery Powered)
- Motor Control

8.1 Connecting to I²C BUS using Pull-Up Resistors

The SCL and SDA pins of the MCP47X6 devices are open-drain configurations. These pins require a pull-up resistor as shown in Figure 8-2.

The pull-up resistor values (R1 and R2) for SCL and SDA pins depend on the operating speed (standard, fast, and high speed) and loading capacitance of the I²C bus line. A higher value of the pull-up resistor consumes less power, but increases the signal transition time (higher RC time constant) on the bus line. Therefore, it can limit the bus operating speed. The lower resistor value, on the other hand, consumes higher power, but allows higher operating speed. If the bus line has higher capacitance due to long metal traces or multiple device connections to the bus line, a smaller pull-up resistor is needed to compensate the long RC time constant. The pull-up resistor is typically chosen between 1 kΩ and 10 kΩ ranges for Standard and Fast modes, and less than 1 kΩ for High-Speed mode.

8.1.1 DEVICE CONNECTION TEST

The user can test the presence of the device on the I²C bus line using a simple I²C command. This test can be achieved by checking an acknowledge response from the device after sending a Read or Write command. Figure 8-1 shows an example with a Read command. The steps are:

a) Set the R/W bit “High” in the device’s address byte.

b) Check the ACK bit of the address byte. If the device acknowledges (ACK = 0) the command, then the device is connected, otherwise it is not connected.

c) Send Stop bit.

FIGURE 8-1: I²C Bus Connection Test.
8.2 Power Supply Considerations

The power source should be as clean as possible. The power supply to the device is also used for the DAC voltage reference internally if the internal VDD is selected as the resistor ladder’s reference voltage (VREF1:VREF0 = 0 0 or 0 1).

Any noise induced on the VDD line can affect the DAC performance. Typical applications will require a bypass capacitor in order to filter out high-frequency noise on the VDD line. The noise can be induced onto the power supply’s traces or as a result of changes on the DAC output. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-2 shows an example of using two bypass capacitors (a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor) in parallel on the VDD line. These capacitors should be placed as close to the VDD pin as possible (within 4 mm). If the application circuit has separate digital and analog power supplies, the VDD and VSS pins of the device should reside on the analog plane.

**Figure 8-2:** Example MCP47X6 Circuit with SOT-23 package.

- **(a) Circuit when VDD is selected as reference**
  (Note: VDD is connected to the reference circuit internally.)

- **(b) Circuit when external reference is used.**

  R1 and R2 are I²C™ pull-up resistors:

  R1 and R2:
  - 5 kΩ - 10 kΩ for fSCL = 100 kHz to 400 kHz
  - ~700Ω for fSCL = 3.4 MHz

  C1: 0.1 µF capacitor Ceramic
  C2: 10 µF capacitor Tantalum
  C3: ~0.1 µF Optional to reduce noise in VOUT pin.
  C4: 0.1 µF capacitor Ceramic
  C5: 10 µF capacitor Tantalum

  **Note:** Pin assignment is opposite in DFN-6 package.
8.3 Application Examples

The MCP47X6 devices are rail-to-rail output DACs designed to operate with a \( V_{DD} \) range of 2.7V to 5.5V. The internal output op amplifier is robust enough to drive common, small-signal loads directly, thus eliminating the cost and size of external buffers for most applications. The user can use gain of 1 or 2 of the output op amplifier by setting the Configuration register bits. Also, the user can use internal \( V_{DD} \) as the reference or use external reference. Various user options and easy-to-use features make the devices suitable for various modern DAC applications.

Application examples include:
- Decreasing Output Step Size
- Building a “Window” DAC
- Bipolar Operation
- Selectable Gain and Offset Bipolar Voltage Output
- Designing a Double-Precision DAC
- Building Programmable Current Source
- Serial Interface Communication Times
- Software I2C Interface Reset Sequence
- Power Supply Considerations
- Layout Considerations

8.3.1 DC SET POINT OR CALIBRATION

A common application for the devices is a digitally-controlled set point and/or calibration of variable parameters, such as sensor offset or slope. For example, the MCP4726 provides 4096 output steps. If voltage reference is 4.096V, the LSb size is 1 mV. If a smaller output step size is desired, a lower external voltage reference is needed.

8.3.1.1 Decreasing Output Step Size

If the application is calibrating the bias voltage of a diode or transistor, a bias voltage range of 0.8V may be desired with about 200 µV resolution per step. Two common methods to achieve small step size are using lower \( V_{REF} \) pin voltage or using a voltage divider on the DAC’s output.

Using an external voltage reference (\( V_{REF} \)) is an option, if the external reference is available with the desired output voltage range. However, occasionally, when using a low-voltage reference voltage, the noise floor causes a SNR error that is intolerable. Using a voltage divider method is another option, and provides some advantages when external voltage reference needs to be very low, or when the desired output voltage is not available. In this case, a larger value reference voltage is used, while two resistors scale the output range down to the precise desired level.

Figure 8-3 illustrates this concept. A bypass capacitor on the output of the voltage divider plays a critical function in attenuating the output noise of the DAC and the induced noise from the environment.

![Figure 8-3: Example Circuit Of Set Point or Threshold Calibration.](image)

**EQUATION 8-1: \( V_{OUT} \) AND \( V_{TRIP} \) CALCULATIONS**

\[
V_{OUT} = V_{REF} \cdot G \cdot \frac{DAC \ Register \ Value}{2^N}
\]

\[
V_{trip} = V_{OUT} \left( \frac{R_2}{R_1 + R_2} \right)
\]
8.3.1.2 Building a “Window” DAC

When calibrating a set point or threshold of a sensor, typically only a small portion of the DAC output range is utilized. If the LSb size is adequate enough to meet the application’s accuracy needs, the unused range is sacrificed without consequences. If greater accuracy is needed, then the output range will need to be reduced to increase the resolution around the desired threshold.

If the threshold is not near \( V_{REF} \), \( 2 \cdot V_{REF} \), or \( V_{SS} \), then creating a “window” around the threshold has several advantages. One simple method to create this “window” is to use a voltage divider network with a pull-up and pull-down resistor. Figure 8-4 and Figure 8-6 illustrate this concept.

![Figure 8-4: Single-Supply “Window” DAC.](image)

**Equation 8-2:** \( V_{OUT} \) and \( V_{TRIP} \) Calculations

\[
V_{OUT} = V_{REF} \cdot G \cdot \frac{DAC \ Register \ Value}{2^N}
\]

\[
V_{TRIP} = \frac{V_{OUT} R_{23} + V_{CC} R_I}{R_1 + R_{23}}
\]

Thevenin Equivalent

\[
R_{23} = \frac{R_2 R_3}{R_2 + R_3}
\]

\[
V_{TRIP} = \frac{(V_{CC} + V_2) + (V_{CC} - V_2)}{R_2 + R_3}
\]

\[
V_{OUT} = V_{TRIP} \frac{R_2}{R_{23}}
\]

8.4 Bipolar Operation

Bipolar operation is achievable by utilizing an external operational amplifier. This configuration is desirable due to the wide variety and availability of op amps. This allows a general purpose DAC, with its cost and availability advantages, to meet almost any desired output voltage range, power and noise performance.

Figure 8-5 illustrates a simple bipolar voltage source configuration. \( R_1 \) and \( R_2 \) allow the gain to be selected, while \( R_3 \) and \( R_4 \) shift the DAC’s output to a selected offset. Note that \( R_4 \) can be tied to \( V_{DD} \), instead of \( V_{SS} \), if a higher offset is desired.

![Figure 8-5: Digitally-Controlled Bipolar Voltage Source Example Circuit.](image)

**Equation 8-3:** \( V_{OUT} \), \( V_{OA+} \), and \( V_O \) Calculations

\[
V_{OUT} = V_{REF} \cdot G \cdot \frac{DAC \ Register \ Value}{2^N}
\]

\[
V_{OA+} = \frac{V_{OUT} \cdot R_4}{R_3 + R_4}
\]

\[
V_O = V_{OA+} \cdot \left(1 + \frac{R_2}{R_1}\right) - V_{DD} \cdot \left(\frac{R_2}{R_1}\right)
\]
8.5 Selectable Gain and Offset Bipolar Voltage Output

In some applications, precision digital control of the output range is desirable. Figure 8-6 illustrates how to use the DAC devices to achieve this in a bipolar or single-supply application.

This circuit is typically used for linearizing a sensor whose slope and offset varies.

The equation to design a bipolar “window” DAC would be utilized if R3, R4 and R5 are populated.

8.5.1 Bipolar DAC Example Using MCP4726

An output step size of 1 mV, with an output range of ±2.05V, is desired for a particular application.

**Step 1:** Calculate the range: +2.05V – (-2.05V) = 4.1V.

**Step 2:** Calculate the resolution needed:

\[ \frac{4.1V}{1 \text{ mV}} = 4100 \]

Since \(2^{12} = 4096\), 12-bit resolution is desired.

**Step 3:** The amplifier gain \((R_2/R_1)\), multiplied by full-scale \(V_{OUT}\) (4.096V), must be equal to the desired minimum output to achieve bipolar operation. Since any gain can be realized by choosing resistor values \((R_1+R_2)\), the \(V_{REF}\) value must be selected first. If a \(V_{REF}\) of 4.096V is used, solve for the amplifier’s gain by setting the DAC to 0, knowing that the output needs to be -2.05V.

The equation can be simplified to:

\[ \frac{-R_2}{R_1} = \frac{-2.05}{4.096V} \]

\[ \frac{R_2}{R_1} = \frac{1}{2} \]

If \(R_1 = 20 \text{ k}\Omega\) and \(R_2 = 10 \text{ k}\Omega\), the gain will be 0.5.

**Step 4:** Next, solve for \(R_3\) and \(R_4\) by setting the DAC to 4096, knowing that the output needs to be +2.05V.

\[ \frac{R_2}{(R_3 + R_4)} = \frac{2.05V + (0.5 \cdot 4.096V)}{1.5 \cdot 4.096V} = \frac{2}{3} \]

If \(R_4 = 20 \text{ k}\Omega\), then \(R_3 = 10 \text{ k}\Omega\)

**Figure 8-6:** Bipolar Voltage Source with Selectable Gain and Offset.

**Equation 8-4:** \(V_{OUT}, V_{OA+}, \text{ and } V_O\) Calculations

\[ V_{OUT} = \frac{V_{REF} \cdot G \cdot \text{DAC Register Value}}{2^N} \]

\[ V_{OA+} = \frac{V_{OUT} \cdot R_4 + V_{CC-} \cdot R_5}{R_3 + R_4} \]

\[ V_O = V_{OA+} \cdot \left(1 + \frac{R_2}{R_1}\right) - V_{IN} \cdot \left(\frac{R_2}{R_1}\right) \]

Offset Adjust  Gain Adjust

**Equation 8-5:** Bipolar “Window” DAC Using \(R_4\) and \(R_5\)

**Thevenin Equivalent**

\[ V_{45} = \frac{V_{CC+} \cdot R_4 + V_{CC-} \cdot R_5}{R_4 + R_5} \]

\[ V_{IN+} = \frac{V_{OUT} \cdot R_4 \cdot R_5}{R_3 + R_4} \]

\[ R_{45} = \frac{R_4 \cdot R_5}{R_4 + R_5} \]

\[ V_O = V_{IN+} \cdot \left(1 + \frac{R_2}{R_1}\right) - V_{IN} \cdot \left(\frac{R_2}{R_1}\right) \]

Offset Adjust  Gain Adjust
8.6 Designing a Double-Precision DAC

Figure 8-7 shows an example design of a single-supply voltage output capable of up to 24-bit resolution. This requires two 12-bit DACs. This design is simply a voltage divider with a buffered output.

As an example, if a similar application to the one developed in Section 8.5.1 “Bipolar DAC Example Using MCP4726” required a resolution of 1 µV instead of 1 mV, and a range of 0V to 4.1V, then 12-bit resolution would not be adequate.

Step 1: Calculate the resolution needed:

\[
\frac{4.1V}{1 \mu V} = 4.1 \times 10^6.
\]

Since \(2^{22} = 4.2 \times 10^6\), 22-bit resolution is desired. Since DNL = ±0.75 LSb, this design can be attempted with the 12-bit DAC.

Step 2: Since DACB’s VOUTB has a resolution of 1 mV, its output only needs to be “pulled” 1/1000 to meet the 1 µV target. Dividing VOUTA by 1000 would allow the application to compensate for DACB’s DNL error.

Step 3: If R2 is 100Ω, then R1 needs to be 100 kΩ.

Step 4: The resulting transfer function is shown in the equation of Example 8-6.

\[
V_{OUT} = \frac{V_{OA} \times R_2 + V_{OB} \times R_1}{R_1 + R_2}
\]

Where:

\[
V_{OA} = \frac{(V_{REF} \times G \times DAC A \ Register \ Value)}{4096}
\]

\[
V_{OB} = \frac{(V_{REF} \times G \times DAC B \ Register \ Value)}{4096}
\]

G = Selected Op Amp Gain

8.7 Building Programmable Current Source

Figure 8-8 shows an example of building a programmable current source using a voltage follower. The current sensor resistor is used to convert the DAC voltage output into a digitally-selectable current source.

The smaller RSENSE is, the less power dissipated across it. However, this also reduces the resolution that the current can be controlled.
8.8 Serial Interface Communication Times

Table 8-1 shows time/frequency of the supported operations of the I²C serial interface for the different serial interface operational frequencies. This, along with the \( V_{OUT} \) output performance (such as slew rate), would be used to determine your application’s volatile DAC register update rate.

**TABLE 8-1: SERIAL INTERFACE TIMES / FREQUENCIES**

<table>
<thead>
<tr>
<th>Code</th>
<th>Function</th>
<th>Writes Volatile Memory?</th>
<th>Writes EEPROM Memory?</th>
<th># of Serial Interface Bits (2)</th>
<th>Command Time (uS)</th>
<th>Command Frequency (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Config., DAC</td>
<td>Config., DAC</td>
<td></td>
<td>100 kHz 400 kHz 3.4 MHz</td>
<td>100 kHz 400 kHz 3.4 MHz</td>
</tr>
<tr>
<td>0 0 X</td>
<td>Write Volatile DAC</td>
<td>Yes(1)</td>
<td>No</td>
<td>No</td>
<td>29</td>
<td>290 72.5 8.5</td>
</tr>
<tr>
<td>0 1 0</td>
<td>Write Volatile Memory</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>38</td>
<td>380 95 11.2</td>
</tr>
<tr>
<td>0 1 1</td>
<td>Write All Memory</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>38</td>
<td>380 95 11.2</td>
</tr>
<tr>
<td>1 0 0</td>
<td>Write NV Configuration</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>20</td>
<td>200 50 5.9</td>
</tr>
<tr>
<td>N/A</td>
<td>Read</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>77</td>
<td>750 187.5 22.1</td>
</tr>
</tbody>
</table>

Note 1: Only the volatile PD1:PD0 bits of the Configuration bits are written.

2: Includes the Start or Stop bits.
8.9 Software $\text{i}^2\text{C}$ Interface Reset Sequence

At times, it may become necessary to perform a Software Reset Sequence to ensure the MCP47X6 device is in a correct and known $\text{i}^2\text{C}$ interface state. This technique only resets the $\text{i}^2\text{C}$ state machine.

This is useful if the MCP47X6 device powers up in an incorrect state (due to excessive bus noise, etc), or if the master device is reset during communication. Figure 8-9 shows the communication sequence to software reset the device.

![Software Reset Sequence Format](image)

The 1st Start bit will cause the device to reset from a state in which it is expecting to receive data from the master device. In this mode, the device is monitoring the data bus in Receive mode and can detect if the Start bit forces an internal Reset.

The nine bits of ‘1’ are used to force a Reset of those devices that could not be reset by the previous Start bit. This occurs only if the MCP47X6 is driving an $A$ bit on the $\text{i}^2\text{C}$ bus, or is in Output mode (from a Read command) and is driving a data bit of ‘0’ onto the $\text{i}^2\text{C}$ bus. In both of these cases, the previous Start bit could not be generated due to the MCP47X6 holding the bus low. By sending out nine ‘1’ bits, it is ensured that the device will see an $A$ bit (the master device does not drive the $\text{i}^2\text{C}$ bus low to acknowledge the data sent by the MCP47X6), which also forces the MCP47X6 to reset.

The 2nd Start bit is sent to address the rare possibility of an erroneous write. This could occur if the master device was reset while sending a Write command to the MCP47X6, AND then as the master device returns to normal operation and issues a Start condition, while the MCP47X6 is issuing an acknowledge. In this case, if the 2nd Start bit is not sent (and the Stop bit was sent) the MCP47X6 could initiate a write cycle.

The Stop bit terminates the current $\text{i}^2\text{C}$ bus activity. The MCP47X6 waits to detect the next Start condition.

This sequence does not effect any other $\text{i}^2\text{C}$ devices which may be on the bus, as they should disregard this as an invalid command.
8.10 Design Considerations

In the design of a system with the MCP4706/4716/4726 devices, the following considerations should be taken into account:

- Power Supply Considerations
- Layout Considerations

8.10.1 POWER SUPPLY CONSIDERATIONS

The typical application will require a bypass capacitor in order to filter high-frequency noise, which can be induced onto the power supply's traces. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-10 illustrates an appropriate bypass strategy.

In this example, the recommended bypass capacitor value is 0.1 µF. This capacitor should be placed as close (within 4 mm) to the device power pin (VDD) as possible.

The power source supplying these devices should be as clean as possible. If the application circuit has separate digital and analog power supplies, VDD and VSS should reside on the analog plane.

8.10.2 LAYOUT CONSIDERATIONS

Several layout considerations may be applicable to your application. These may include:

- Noise
- PCB Area Requirements

8.10.2.1 Noise

Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP47X6's performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR). Multi-layer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing. Particularly harsh environments may require shielding of critical signals.

Separate digital and analog ground planes are recommended. In this case, the VSS pin and the ground pins of the VDD capacitors should be terminated to the analog ground plane.

Note: Breadboards and wire-wrapped boards are not recommended.

8.10.2.2 PCB Area Requirements

In some applications, PCB area is a criteria for device selection. Table 8-2 shows the typical package dimensions and area for the different package options. The table also shows the relative area factor compared to the smallest area. For space critical applications, the DFN package would be the suggested package.

<table>
<thead>
<tr>
<th>Package</th>
<th>Pins</th>
<th>Type</th>
<th>Code</th>
<th>Dimensions (mm)</th>
<th>Area (mm²)</th>
<th>Relative Area</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>6</td>
<td>SOT-23</td>
<td>CH</td>
<td>Length 2.90, Width 2.70</td>
<td>7.83</td>
<td>1.96</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>DFN</td>
<td>MAY</td>
<td>Length 2.00, Width 2.00</td>
<td>4.00</td>
<td>1</td>
</tr>
</tbody>
</table>

Note 1: Does not include recommended land pattern dimensions. Dimensions are typical values.
9.0 DEVELOPMENT SUPPORT

Development support can be classified into two groups. These are:

- Development Tools
- Technical Documentation

9.1 Development Tools

Several development tools are available to assist in your design and evaluation of the MCP47X6 devices. The currently available tools are shown in Table 9-1.

These boards may be purchased directly from the Microchip web site at www.microchip.com.

9.1.1 MCP47X6 PICtail™ PLUS DAUGHTER BOARD

The MCP47X6 PICtail™ Plus Daughter Board (order number: ADM00317) is available from Microchip Technology Inc. This board works with Microchip’s PICkit™ Serial Analyzer and PIC® Explorer 16 Development Board. The firmware example is also available for the Explorer 16 Development Board with PIC24FJ128.

Figure 9-1 shows the MCP47X6 PICtail™ Plus Daughter Board being used with a PIC® Explorer 16 Development Board (order number: ADM00317), while Figure 9-2 shows the MCP47X6 PICtail™ Plus Daughter Board being used with a PICkit™ Serial Analyzer. The PICkit™ Serial Analyzer allows the user to quickly evaluate the DAC operation. Refer to the “MCP47X6 PICtail™ Plus Daughter Board User’s Guide” (DS51932) for detailed descriptions on operating the daughter board.

Refer to www.microchip.com for further information on this product and related material for the users.

**TABLE 9-1: DEVELOPMENT TOOLS**

<table>
<thead>
<tr>
<th>Board Name</th>
<th>Part #</th>
<th>Supported Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board</td>
<td>SC70EV</td>
<td>MCP4706, MCP4716, MCP4726</td>
</tr>
<tr>
<td>MCP47X6 PICtail™ Plus Daughter Board Evaluation Board$^{(1,2)}$</td>
<td>ADM00317</td>
<td>MCP47X6</td>
</tr>
</tbody>
</table>

**Note 1:** Requires a PICDEM™ Demo board. See the User’s Guide for additional information and requirements.

**2:** Requires a PICkit™ Serial Analyzer. See the User’s Guide for additional information and requirements.
9.2 Technical Documentation

Several additional technical documents are available to assist you in your design and development. These technical documents include Application Notes, Technical Briefs, and Design Guides. Table 9-2 shows some of these documents.

**TABLE 9-2: TECHNICAL DOCUMENTATION**

<table>
<thead>
<tr>
<th>Application Note Number</th>
<th>Title</th>
<th>Literature #</th>
</tr>
</thead>
<tbody>
<tr>
<td>AN1326</td>
<td>Using the MCP4728 12-Bit DAC for LDMOS Amplifier Bias Control Applications</td>
<td>DS01326</td>
</tr>
<tr>
<td>—</td>
<td>Signal Chain Design Guide</td>
<td>DS21825</td>
</tr>
<tr>
<td>—</td>
<td>Analog Solutions for Automotive Applications Design Guide</td>
<td>DS01005</td>
</tr>
</tbody>
</table>
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

**6-Lead SOT-23**

![6-Lead SOT-23 Example]

<table>
<thead>
<tr>
<th>Address Option</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0 (00)</td>
<td>DBNN</td>
</tr>
<tr>
<td>A1 (01)</td>
<td>DCNN</td>
</tr>
<tr>
<td>A2 (10)</td>
<td>DDNN</td>
</tr>
<tr>
<td>A3 (11)</td>
<td>DENN</td>
</tr>
</tbody>
</table>

**6-Lead DFN (2x2x0.9 mm)**

![6-Lead DFN Example]

<table>
<thead>
<tr>
<th>Address Option</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0 (00)</td>
<td>AAA</td>
</tr>
<tr>
<td>A1 (01)</td>
<td>AAB</td>
</tr>
<tr>
<td>A2 (10)</td>
<td>AAC</td>
</tr>
<tr>
<td>A3 (11)</td>
<td>AAD</td>
</tr>
</tbody>
</table>

**Legend:**
- **XX...X** Customer-specific information
- **Y** Year code (last digit of calendar year)
- **YY** Year code (last 2 digits of calendar year)
- **WWW** Week code (week of January 1 is week '01')
- **NNN** Alphanumeric traceability code
- **(e3)** Pb-free JEDEC designator for Matte Tin (Sn)
- ***Pb-free** This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Outside Lead Pitch</td>
<td>e1</td>
</tr>
<tr>
<td>Overall Height</td>
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</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
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</tr>
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<td>Overall Length</td>
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<tr>
<td>Foot Length</td>
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</tr>
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</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

**Notes:**
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B
6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

**Recommended Land Pattern**

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
</tr>
<tr>
<td>Contact Pad Width (X6)</td>
<td>X</td>
</tr>
<tr>
<td>Contact Pad Length (X6)</td>
<td>Y</td>
</tr>
<tr>
<td>Distance Between Pads</td>
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<td>Overall Width</td>
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**Notes:**
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
6-Lead Plastic Dual Flat, No Lead Package (MA[Y]) - 2x2x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/package
6-Lead Plastic Dual Flat, No Lead Package (MA[Y]) - 2x2x0.9mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

![Diagram of MCP4706/4716/4726 package](image)

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<td>Contact Thickness</td>
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<td>Overall Length</td>
<td>D</td>
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<td>Overall Width</td>
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<tr>
<td>Exposed Pad Length</td>
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<tr>
<td>Exposed Pad Width</td>
<td>E2</td>
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<tr>
<td>Contact Width</td>
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<tr>
<td>Contact Length</td>
<td>L</td>
</tr>
<tr>
<td>Contact-to-Exposed Pad</td>
<td>K</td>
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**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension, Theoretically exact value shown without tolerances,
   - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-120C Sheet 2 of 2
6-Lead Plastic Dual Flat, No Lead Package (MA) - 2x2x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packing

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<td>Optional Center Pad Length</td>
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Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2120A
APPENDIX A: REVISION HISTORY

Revision C (April 2012)
The following is the list of modifications:
1. Updated the layout of the Absolute Maximum Rating page.
2. Added three new sections, Section 4.4.3 “Output Slew Rate”, Section 4.4.4 “Small Capacitive Load” and Section 4.4.5 “Large Capacitive Load”.
3. Enhanced former Section 4.4.3 (now Section 4.4.6 “Driving Resistive and capacitive Loads”).
4. Updated the descriptive information related to the ACK bit in FIGURE 6-5: “Read Command Format for 12-bit DAC (MCP4726) and 10-bit DAC (MCP4716).”
5. Corrected DFN package code and drawings to MAY code (from MA code). Both MA and MAY have the same dimensions/footprint.

Revision B (September 2011)
The following is the list of modifications:
1. Updated references to graphics and equations in the text.
2. Updated notes in FIGURE 6-6: “Read Command Format for 8-bit DAC (MCP4706).”

Revision A (February 2011)
• Original Release of this Document.
PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

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<th>PART NO.</th>
<th>Device</th>
<th>Address Options</th>
<th>Tape and Reel</th>
<th>Temperature Range</th>
<th>Package</th>
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<td>X / XX</td>
<td>MCP4706: Single Channel 8-Bit DAC with EEPROM Memory</td>
<td>A0 = &quot;1100000&quot; I²C Address.</td>
<td>Devices ordered from the Microchip Sample center will have this address.</td>
<td>E = -40°C to +125°C</td>
<td>CH = Plastic Small Outline Transistor (SOT-23-6), 6-lead</td>
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<td>MCP4716: Single Channel 10-Bit DAC with EEPROM Memory</td>
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<td>A4 = &quot;1100100&quot; I²C Address.</td>
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<td>A5 = &quot;1100101&quot; I²C Address.</td>
<td>A6 = &quot;1100110&quot; I²C Address.</td>
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<td>A7 = &quot;1100111&quot; I²C Address.</td>
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Examples:

a) MCP4706A0T-E/CH: 8-bit V_OUT resolution, I²C Address "1100000", Tape and Reel, Extended Temp., 6LD SOT-23 pkg.
b) MCP4706A6T-E/CH: 8-bit V_OUT resolution, I²C Address "1100110", Tape and Reel, Extended Temp., 6LD SOT-23 pkg.
c) MCP4706A0T-E/MAY: 8-bit V_OUT resolution, I²C Address "1100000", Tape and Reel, Extended Temp., 6LD DFN pkg.
d) MCP4706A6T-E/MAY: 8-bit V_OUT resolution, I²C Address "1100110", Tape and Reel, Extended Temp., 6LD DFN pkg.

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DS22272C-page 83
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